




Description

Vectron's VC-801 Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VC-801 uses fundamental or 3rd overtone crystals resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

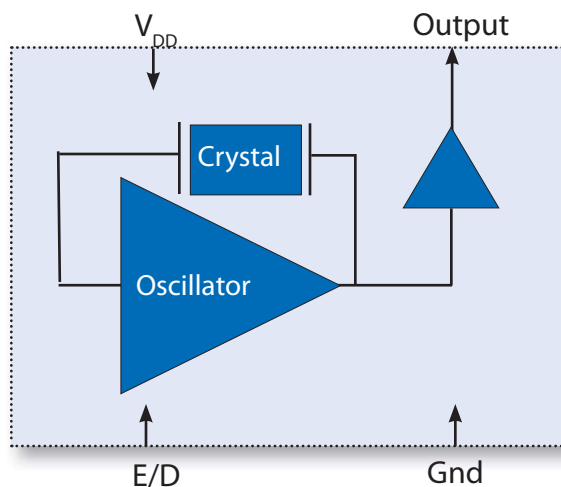
Features

- CMOS output XO
- Output Frequencies from 1.544 MHz to 125.000 MHz
- 5.0, 3.3, 2.5 or 1.8 V Operation
- Low Jitter Performance
- Output Disable Feature
- Excellent 20ppm temperature stability,
- -10/70°C or -40/85°C operating temperature
- Small Industry Standard Package, 3.2.0x5.0x1.3mm
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Fiber Channel
- Digital Video
- Broadband Access
- Base Stations, Picocells

Block Diagram



Specifications

Table 1. Electrical Performance, 5V Option

| Parameter | Symbol | Min | Typical | Maximum | Units |
|--|--|-------------------------------|-----------|----------------|--------------------|
| Supply | | | | | |
| Voltage ¹ | V_{DD} | 4.5 | 5.0 | 5.5 | V |
| Max Voltage | | -0.7 | | 7 | V |
| Current ² ≤20.000MHz 20.001 to 50.000MHz 50.001 to 75.000MHz | I_{DD} | | | 10 30 40 | mA |
| Current, Output Disabled | | | | 30 | uA |
| Frequency | | | | | |
| Nominal Frequency ³ | f_N | 1.544 | | 75.000 | MHz |
| Stability ⁴ , (Ordering Option) | | ±20, ±25, ±32, ±50, ±100 | | | ppm |
| Outputs | | | | | |
| Output Logic Levels ² Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive | V_{OH} V_{OL} I_{OH} I_{OL} | 0.9* V_{DD} 16 16 | | 0.1* V_{DD} | V V mA mA |
| Load | I_{OUT} | | | 15 | pF |
| Output Rise /Fall Time ² <20.000MHz 20.000 to 50.000MHz 50.001 to 75.000MHz | t_R/t_F | | | 8 5 2 | ns |
| Output Leakage, Output Disabled | I_z | | | ±10 | uA |
| Duty Cycle ^{2,5} | | 45 | 50 | 55 | % |
| Period Jitter ⁶ RMS Peak-Peak | ϕ_J | | 3.0 21 | | ps |
| RMS Jitter, 12k-20MHz | ϕ_J | | 0.5 | 1 | ps |
| Enable/Disable | | | | | |
| Output Enable/Disable ⁷ Output Enable Output Disable | V_{IH} V_{IL} | 4.0 | | 0.8 | V V |
| Disable time | t_D | | | 100 | ns |
| Enable Internal Pull-Up Resistor | | | 100 | | Kohm |
| Start-Up Time | t_{SU} | | | 8 | ms |
| Operating Temp, (Ordering Option) | T_{OP} | -10/70 or -40/85 | | | °C |

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.
- 2] Parameters are tested with production test circuit, Figure 1.
- 3] See Standard Frequencies and Ordering Information tables for more specific information.
- 4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging for 50 and 100ppm options.
- 5] Duty Cycle is measured as On Time/Period (Fig 2).
- 6] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.
- 7] The Output is Enabled if the Enable/Disable is left open.

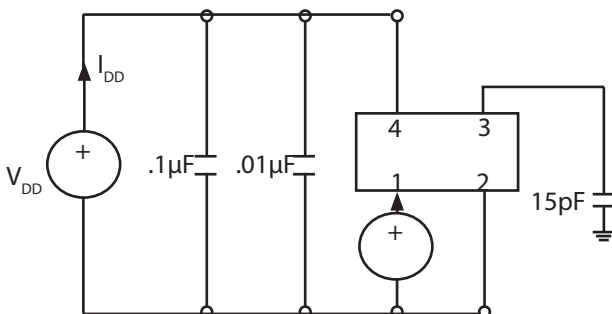


Fig 1: Test Circuit

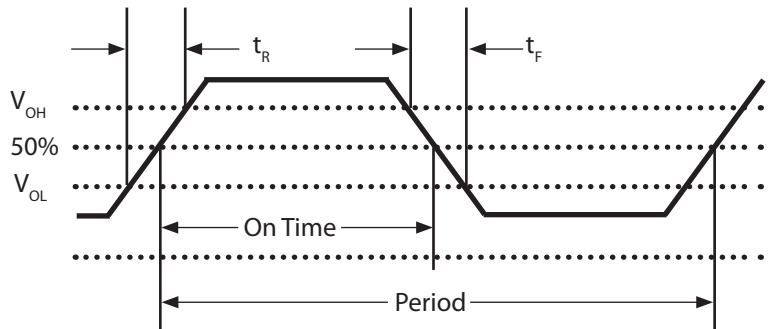


Fig 2: Waveform

Specifications

Table 2. Electrical Performance, 3.3V Option

| Parameter | Symbol | Min | Typical | Maximum | Units |
|--|--|-----------------------------|-----------|---------------------|--------------------|
| Supply | | | | | |
| Voltage ¹ | V_{DD} | 2.97 | 3.3 | 3.63 | V |
| Maximum Voltage | | -0.5 | | 5 | V |
| Current ² ≤20.000MHz 20.001 to 50.000MHz 50.001 to 75.000MHz 75.001 to 125.000MHz | I_{DD} | | | 7 20 30 40 | mA |
| Current, Output Disabled | | | | 30 | uA |
| Frequency | | | | | |
| Nominal Frequency ³ | f_N | 1.544 | | 125.000 | MHz |
| Stability ⁴ , (Ordering Option) | | ±20, ±25, ±32, ±50, ±100 | | | ppm |
| Outputs | | | | | |
| Output Logic Levels ² Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive | V_{OH} V_{OL} I_{OH} I_{OL} | 0.9* V_{DD} 8 8 | | 0.1* V_{DD} | V V mA mA |
| Load | I_{OUT} | | | 15 | pF |
| Output Rise /Fall Time ² <20.000MHz 20.000 to 50.000MHz 50.001 to 125.000MHz | t_R/t_F | | | 10 6 3 | ns |
| Output Leakage, Output Disabled | I_z | | | ±10 | uA |
| Duty Cycle ^{2,5} | | 45 | 50 | 55 | % |
| Period Jitter ⁶ RMS Peak-Peak | ϕJ | | 3.0 21 | | ps |
| RMS Jitter, Peak - Peak | ϕJ | | 0.5 | 1 | ps |
| Enable/Disable | | | | | |
| Output Enable/Disable ⁷ Output Enable Output Disable | V_{IH} V_{IL} | 2.0 | | 0.5 | V V |
| Disable time | t_D | | | 100 | ns |
| Enable Internal Pull-Up Resistor | | | 100 | | Kohm |
| Start-Up Time | t_{SU} | | | 8 | ms |
| Operating Temp, (Ordering Option) | T_{OP} | -10/70 or -40/85 | | | °C |

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01 uF.
- 2] Parameters are tested with production test circuit, Figure 1.
- 3] See Standard Frequencies and Ordering Information tables for more specific information.
- 4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging for 50 and 100ppm options.
- 5] Duty Cycle is measured as On Time/Period (Fig 2).
- 6] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.
- 7] The Output is Enabled if the Enable/Disable is left open.

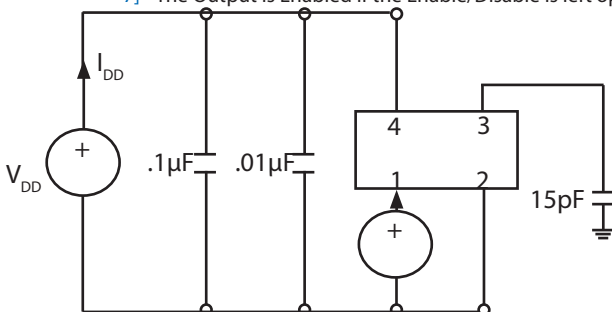


Fig 1: Test Circuit

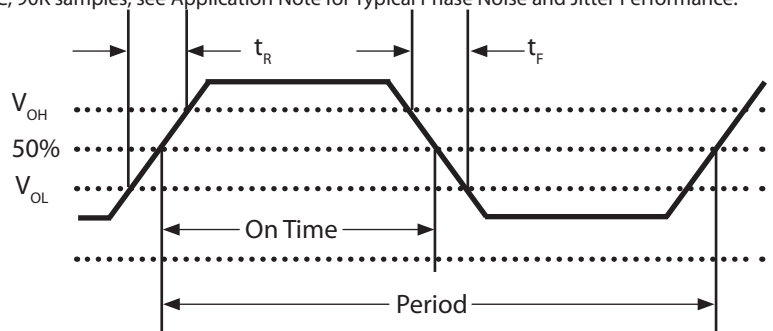


Fig 2: Waveform

Specifications

Table 3. Electrical Performance, 2.5V Option

| Parameter | Symbol | Min | Typical | Maximum | Units |
|---|--|---------------------------------------|-----------|--------------------------|--------------------------------|
| Supply | | | | | |
| Voltage ¹ | V_{DD} | 2.25 | 2.5 | 2.75 | V |
| Maximum Voltage | | -0.5 | | 5 | V |
| Current ² ≤20.000MHz 20.001 to 50.000MHz 50.001 to 75.000MHz 75.001 to 100.000MHz 100.001 to 125.000MHz | I_{DD} | | | 5 7 20 25 30 | mA |
| Current, Output Disabled | | | | 30 | uA |
| Frequency | | | | | |
| Nominal Frequency ³ | f_N | 1.544 | | 125.000 | MHz |
| Stability ⁴ , (Ordering Option) | | ±20, ±25, ±32, ±50, ±100 | | | ppm |
| Outputs | | | | | |
| Output Logic Levels ^{2,3} Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive Output Logic High Drive ⁵ Output Logic Low Drive ⁵ | V_{OH} V_{OL} I_{OH} I_{OL} I_{OH} I_{OL} | 0.9* V_{DD} 4 4 8 8 | | 0.1* V_{DD} | V V mA mA mA mA |
| Load | I_{OUT} | | | 15 | pF |
| Output Rise /Fall Time ² <20.000MHz 20.000 to 50.000MHz 50.001 to 125.000MHz | t_R/t_F | | | 10 6 3 | ns |
| Output Leakage, Output Disabled | I_z | | | ±10 | uA |
| Duty Cycle ^{2,6} | | 45 | 50 | 55 | % |
| Period Jitter ⁷ RMS Peak-Peak | ϕ_J | | 3.0 21 | | ps |
| RMS Jitter, 12k-20MHz | ϕ_J | | 0.5 | 1 | ps |
| Enable/Disable | | | | | |
| Output Enable/Disable ⁸ Output Enable Output Disable | V_{IH} V_{IL} | 1.75 | | 0.5 | V V |
| Disable time | t_D | | | | ns |
| Enable Internal Pull-Up Resistor | | | 100 | | Kohm |
| Start-Up Time | t_{SU} | | | 8 | ms |
| Operating Temp, (Ordering Option) | T_{OP} | -10/70 or -40/85 | | | °C |

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.

2] Parameters are tested with production test circuit, Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging for 50 and 100ppm options.

5] Overtone Designs, Output Frequencies >35Hz.

6] Duty Cycle is measured as On Time/Period (Fig 2).

7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.

8] The Output is Enabled if the Enable/Disable is left open.

Table 4. Electrical Performance, 1.8V Option

| Parameter | Symbol | Min | Typical | Maximum | Units |
|---|--|---|-----------|---------------------|--------------------|
| Supply | | | | | |
| Voltage ¹ | V_{DD} | 1.71 | 1.8 | 1.89 | V |
| Maximum Voltage | | -0.5 | | 3.6 | V |
| Current ² ≤20.000MHz 20.001 to 70.000MHz 70.001 to 100.000MHz 100.001 to 125.000MHz | I_{DD} | | | 5 15 20 25 | mA |
| Current, Output Disabled | | | | 30 | uA |
| Frequency | | | | | |
| Nominal Frequency ³ | f_N | 1.544 | | 125.000 | MHz |
| Stability ⁴ , (Ordering Option) | | ±20, ±25, ±32, ±50, ±100 | | | ppm |
| Outputs | | | | | |
| Output Logic Levels ^{2,3} Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive Output Logic High Drive ⁵ Output Logic Low Drive ⁵ | V_{OH} V_{OL} I_{OH} I_{OL} I_{OH} I_{OL} | 0.9* V_{DD} 2.8 2.8 8 8 | | 0.1* V_{DD} | V V mA mA |
| Load | I_{OUT} | | | 15 | pF |
| Output Rise /Fall Time ² <20.000MHz 20.000 to 50.000MHz 50.001 to 125.000MHz | t_R/t_F | | | 10 6 3 | ns |
| Output Leakage, Output Disabled | I_Z | | | ±10 | uA |
| Duty Cycle ^{2,6} | | 45 | 50 | 55 | % |
| Period Jitter ⁷ RMS Peak-Peak | ϕJ | | 3.0 21 | | ps |
| RMS Jitter, 12kHz-20MHz | ϕJ | | 0.5 | 1 | ps |
| Enable/Disable | | | | | |
| Output Enable/Disable ⁸ Output Enable Output Disable | V_{IH} V_{IL} | 1.26 | | 0.5 | V V |
| Disable time | t_D | | | 100 | ns |
| Enable Internal Pull-Up Resistor | | | 1 | | Mohm |
| Start-Up Time | t_{SU} | | | 8 | ms |
| Operating Temp, Ordering Option | T_{OP} | -10/70 or -40/85 | | | °C |

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01 uF.
- 2] Parameters are tested with production test circuit, Figure 1.
- 3] See Standard Frequencies and Ordering Information tables for more specific information.
- 4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging for 50 and 100ppm options.
- 5] Overtone Designs, Output Frequencies>35MHz.
- 6] Duty Cycle is measured as On Time/Period (Fig 2).
- 7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples, see Application Note for Typical Phase Noise and Jitter Performance.
- 8] The Output is Enabled if the Enable/Disable is left open.

Outline Drawing & Pad Layout

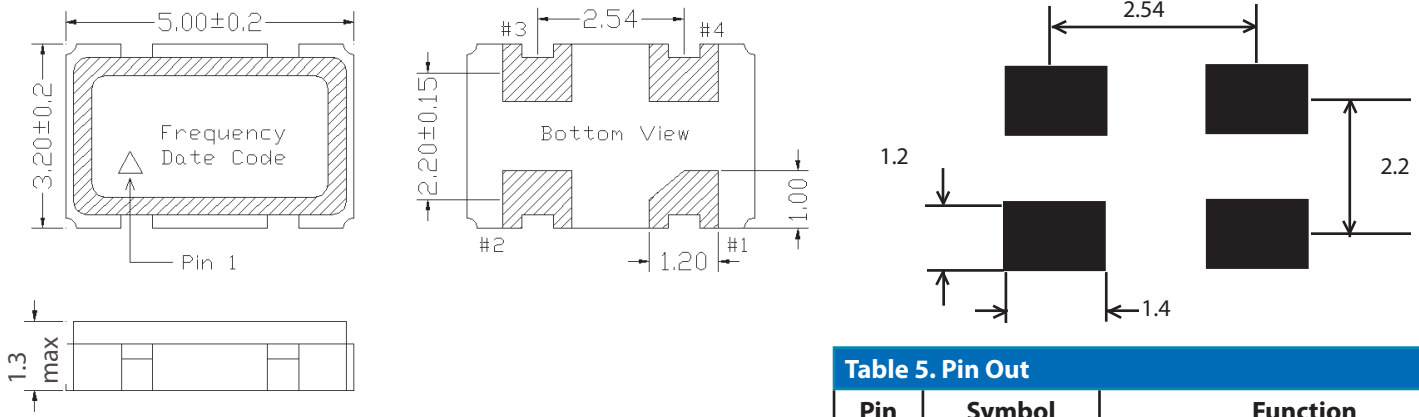


Table 5. Pin Out

| Pin | Symbol | Function |
|-----|-----------------|----------------------------|
| 1 | E/D | Enable Disable |
| 2 | GND | Case and Electrical Ground |
| 3 | Output | Output |
| 4 | V _{DD} | Power Supply Voltage |

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-801 family is capable of meeting the following qualification tests:

Table 6. Environmental Compliance

| Parameter | Conditions |
|----------------------------|--------------------------|
| Mechanical Shock | MIL-STD-883, Method 2002 |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Gross and Fine Leak | MIL-STD-883, Method 1014 |
| Resistance to Solvents | MIL-STD-883, Method 2015 |
| Moisture Sensitivity Level | MSL 1 |
| Contact Pads | Gold over Nickel |

Although ESD protection circuitry has been designed into the VC-801 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 7. ESD Ratings

| Model | Minimum | Conditions |
|----------------------|---------|--------------------------|
| Human Body Model | 1500V | MIL-STD-883, Method 3015 |
| Charged Device Model | 1000V | JESD22-C101 |

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before V_{DD}.

Table 8. Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---------------------|-----------------|------------|----------|
| Storage Temperature | T _S | -55 to 125 | °C |
| Soldering Temp/Time | T _{LS} | 260 / 20 | °C / sec |

IR Reflow

Solderprofile:

The VC-801 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VC-801 device is hermetically sealed so an aqueous wash is not an issue.

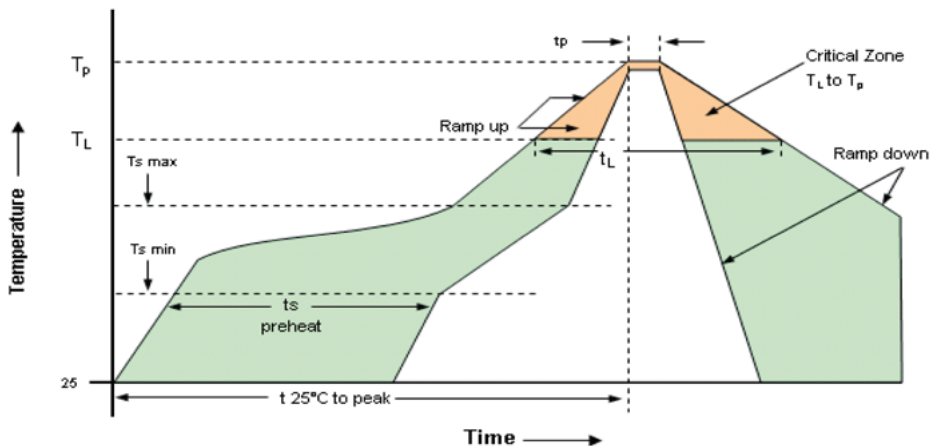


Table 9. Reflow Profile

| Parameter | Symbol | Value |
|--|--------------------|---|
| PreHeat Time T _s -min T _s -max | t _s | 60 sec Min, 260 sec Max 150°C 200°C |
| Ramp Up | R _{UP} | 3 °C/sec Max |
| Time Above 217 °C | t _L | 60 sec Min, 150 sec Max |
| Time To Peak Temperature | T _{AMB-P} | 480 sec Max |
| Time at 260 °C | t _p | 10 sec Max |
| Ramp Down | R _{DN} | 6 °C/sec Max |

Tape and Reel

Table 10 . Tape and Reel Dimensions

| Dimension | Tape Dimensions (mm) | | | | | Reel Dimensions (mm) | | | | | | | |
|-----------|----------------------|-----|-----|-----|-----|----------------------|-----|-----|-----|-----|-----|-----|------------|
| | W | F | Do | Po | P1 | A | B | C | D | N | W1 | W2 | # Per Reel |
| Tolerance | Typ | Typ | Typ | Typ | Typ | Typ | Min | Typ | Min | Min | Typ | Max | |
| VC-801 | 16 | 7.5 | 1.5 | 4 | 8 | 180 | 2 | 13 | 21 | 60 | 17 | 21 | 1000 |

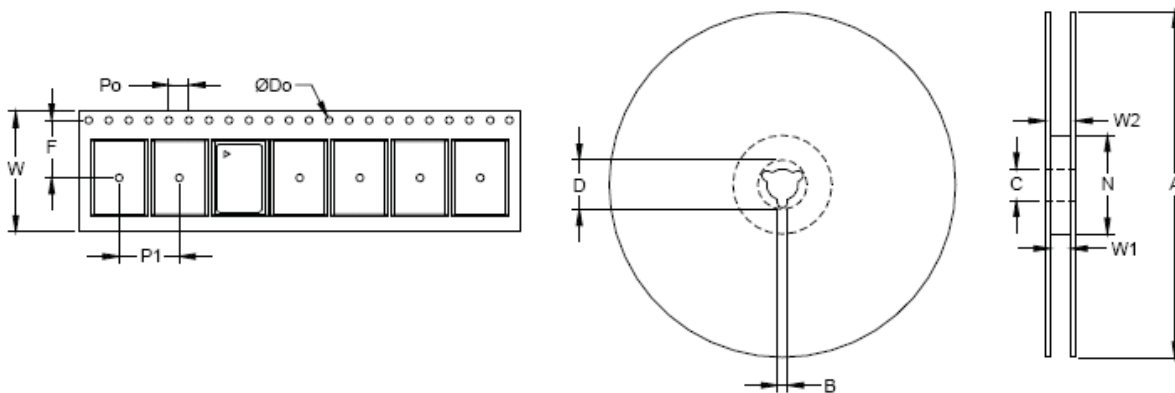
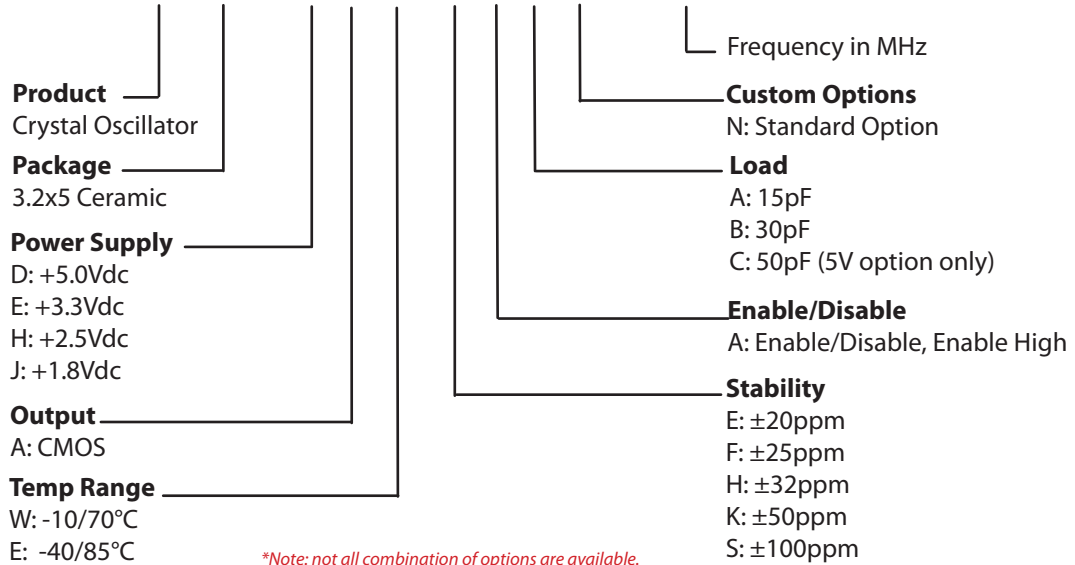


Table 11. Standard Output Frequencies (MHz)

| | | | | | | | |
|--------|-----------|---------|---------|-----------|---------|---------|--------|
| 9.8304 | 10.000 | 11.0590 | 11.0596 | 11.2896 | 12.000 | 12.272 | 12.288 |
| 12.353 | 13.000 | 13.500 | 13.560 | 14.318 | 14.7456 | 16.000 | 16.376 |
| 16.384 | 16.777216 | 16.800 | 17.734 | 17.734475 | 18.432 | 19.440 | 19.660 |
| 19.800 | 20.000 | 20.480 | 22.000 | 22.5792 | 24.000 | 24.5453 | 24.576 |
| 25.000 | 26.000 | 27.000 | 27,120 | 28.686 | 28.375 | 30.000 | 32.000 |
| 32.768 | 33.000 | 33.333 | 34.368 | 36.000 | 37.056 | 47.500 | 40.000 |
| 42.500 | 44.000 | 44.736 | 48.000 | 48.090 | 50.000 | 54.000 | 60.000 |
| 62.500 | 66.000 | 66.666 | 75.000 | 80.000 | 100.000 | 125.000 | |

Ordering Information

VC-801- E A W- K A A N- xxMxxxxxxx



**Note: not all combination of options are available.
Other specifications may be available upon request.*

Example: VC-801-EAW-KAAN-125M000000

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