

Helping Customers Innovate, Improve & Grow

### Features

- 32.768 kHz  $\pm 5$  ppm frequency stability over temp
- Operating temperature ranges: 0°C to +70°C and -40°C to +85°C
- Package: 1.5 x 0.8 mm CSP
- Ultra-low power:  $< 1 \mu\text{A}$
- Vdd supply range: 1.5V to 3.63V
- Improved stability reduces system power with fewer network timekeeping updates
- Internal filtering eliminates external Vdd bypass cap and saves space
- Pb-free, RoHS and REACH compliant

### Applications

- RTC Reference Clock
- Smart Meters (AMR)
- Health and Wellness Monitors
- Pulse-per-Second (pps) Timekeeping
- Wireless BLE Connectivity
- Automotive
- Industrial Controls and Automation

### Performance Specifications

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency and Stability</b>						
Output Frequency	f <sub>out</sub>	32.768			kHz	
Initial Tolerance	F <sub>init</sub>	-5.0	–	5.0	ppm	T <sub>A</sub> =25°C, includes reflow. Tested with Agilent 53132A freq. counter, gate time $\geq 100\text{ms}$ .
Frequency Stability Over Temperature	F <sub>stab</sub>	-5.0		5.0	ppm	Stability part number code = E, includes $\pm 20\%$ load variation
		-10		10		Stability part number code = F, includes $\pm 20\%$ load variation
		-20		20		Stability part number code = 1, includes $\pm 20\%$ load variation
Frequency Stability vs Voltage	F <sub>vdd</sub>	-0.75	–	0.75	ppm	1.8V $\pm 10\%$
		-1.5		1.5		1.5V - 3.63V
First Year Frequency Aging	F <sub>aging</sub>	-1.0		1.0	ppm	T <sub>A</sub> = 25°C, Vdd = 3.0V
<b>Jitter Performance (T<sub>A</sub> = over temp)</b>						
Long Term Jitter				2.5	$\mu\text{spp}$	81920 cycles (2.5 sec), 100 samples
Period Jitter			35		ns <sub>RMS</sub>	N = 10,000, T <sub>A</sub> = 25°C, Vdd = 1.5V - 3.63V
<b>Supply Voltage and Current Consumption</b>						
Operating Supply Voltage	Vdd	1.5		3.63	V	T <sub>A</sub> = -40°C to +85°C
Core Supply Current	I <sub>dd</sub>		0.99		$\mu\text{A}$	T <sub>A</sub> = 25°C, Vdd = 1.8V, LVCMOS Output configuration, No Load
				1.52		T <sub>A</sub> = -40°C to +85°C, Vdd = 1.5V - 3.63V, No Load
Power-Supply Ramp	t <sub>Vdd_Ramp</sub>			100	ms	Vdd Ramp-Up 0 to 90% Vdd, T <sub>A</sub> = -40°C to +85°C
Start-up Time at Power-up	t <sub>start</sub>		200	300	ms	Valid Output with frequency stability specifications
<b>Operating Temperature Range</b>						
Commercial Temperature	Op_Temp	0		70	°C	
Industrial Temperature		-40		85	°C	
<b>LVCMOS Output</b>						
Output Rise/Fall Time	t <sub>r</sub> , t <sub>f</sub>		100	200	ns	10-90%, 15 pF Load
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V - 3.63V. I <sub>OH</sub> = -1 $\mu\text{A}$ , 15 pF Load
Output Voltage Low	vol			10%	v	Vdd: 1.5V - 3.63V. I <sub>OL</sub> = -1 $\mu\text{A}$ , 15 pF Load

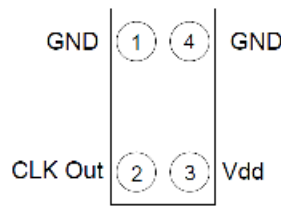
#### Notes:

1. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled, Calculating Load Current.

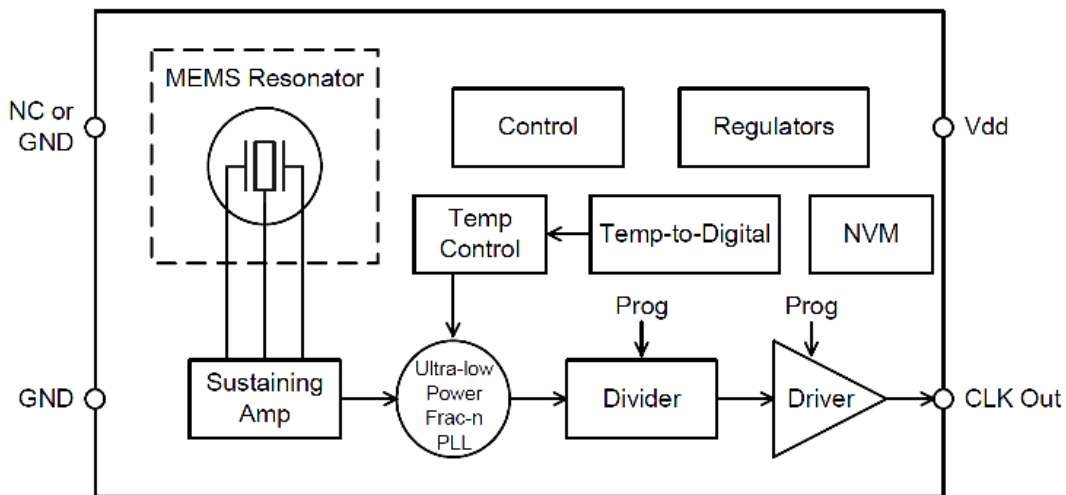
# Pin Functionality

Pin Connections					
SMD Pin	CSP Pin	SOT23-5 Pin	Symbol	I/O	Functionality
1	n/a	2	NC	No Connect	No Connect. Will not respond to any input signal. When interfacing to an MCU's XTAL input pins, this pin is typically connected to the receiving IC's X Out pin. In this case, the MT-9560A will not be affected by the signal on this pin. If not interfacing to an XTAL oscillator, leave pin 1 floating (no connect).
2	1, 4	1, 5	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground. The GND pins on the SOT23 and CSP packages can be connected together, as long as both GND pins are connected ground.
3	2	4	CLK Out	out	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The MT-9560A oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
4	3	3	Vdd	Power Supply	Connect to power supply $1.5V \leq Vdd \leq 3.63V$ . Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). Internal power supply filtering will reject more than 500 mV <sub>pp</sub> with frequency components through 10 MHz. Contact factory for applications that require a wider operating supply voltage range.

CSP Package (Top View)



# Block Diagram



## Absolute Maximum

Attempted operation outside the absolute maximum ratings cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-05 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD22-A115	750	V
Machine Model (MM) ESD Protection	JESD22-C101	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

## Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
1508 CSP	TBD		

## Description

The MT-9560A is an ultra-small and ultra-low power 32.768 kHz TCXO optimized for battery-powered applications. Vectron's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical core supply current is only 1  $\mu$ A.

Vectron's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with a unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, Vectron's MEMS resonator die can be used like any other semiconductor die. One unique result of Vectron's MEMS First and EpiSeal manufacturing processes is the capability to integrate Vectron's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

### TCXO Frequency Stability

The MT-9560A is factory calibrated (trimmed) over multiple frequency points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C<sup>2</sup> temperature coefficient, the MT-9560A temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range.

When measuring the MT-9560A output frequency with a frequency counter, it is important to make sure the counter's gate time is >100ms. The slow frequency of a 32kHz clock will give false readings with faster gate times.

### Power Supply Noise Immunity

In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor to keep the footprint as small as possible. Internal power supply filtering is designed to reject more than 500 mV noise and frequency components from low frequency to more than 10 MHz.

### Start-up and Steady-State Supply Current

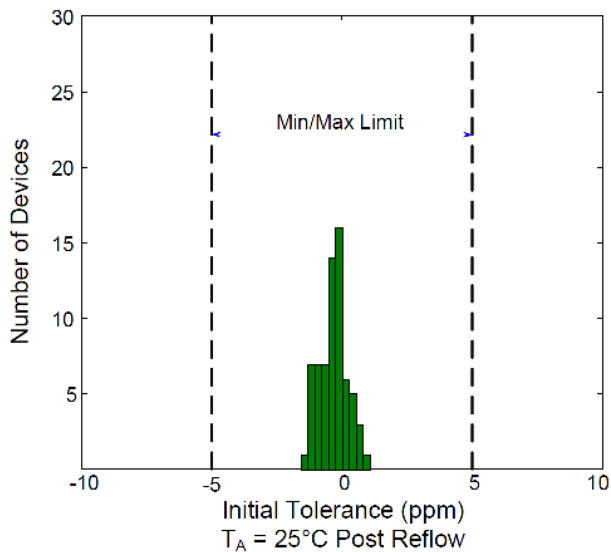
The MT-9560A TCXO starts-up to a valid output frequency within 300 ms (150ms typ). To ensure proper start-up, Vdd power-supply ramp, from a power-down state to 90% of final Vdd, must be less than 100ms.

During initial power-up, the MT-9560A power-cycles internal blocks, as shown in the power-supply start-up and steady state plot in the Typical Operating Curves section. Power-up and initialization is typically 200 ms, and during that time, the peak supply current reaches 28  $\mu$ A as the internal capacitors are charged, then sequentially drops to its 990 nA steady-state current. During steady-state operation, the internal temperature compensation circuit turns on every 350 ms for a duration of approximately 10 ms.

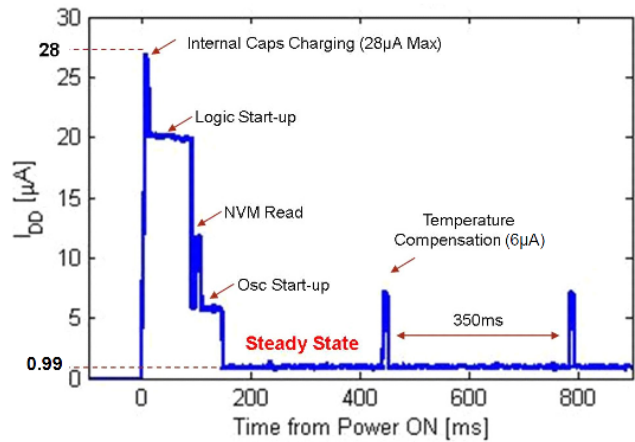
### Output Voltage

The MT-9560A has standard LVCMOS output swing. For DC-coupled applications, output VOH and VOL are individually factory programmed to the customers' requirement. VOH programming range is between 600 mV and 1.225V in 100 mV increments. Similarly, VOL programming range is between 350 mV and 800 mV. For example; a PMIC or MCU is internally 1.8V logic compatible, and requires a 1.2V VIH and a 0.6V VIL.

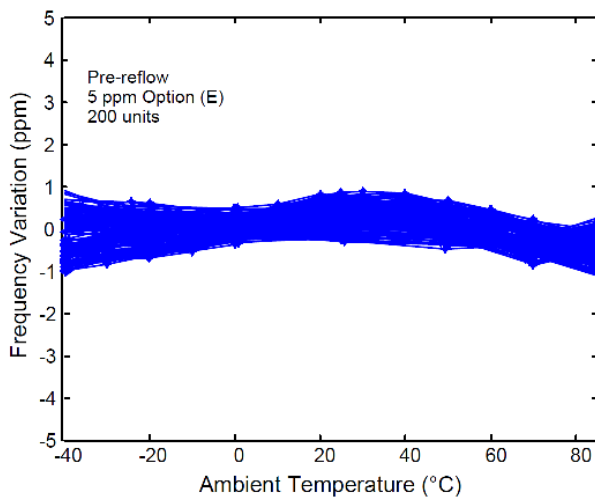
Initial Tolerance Histogram



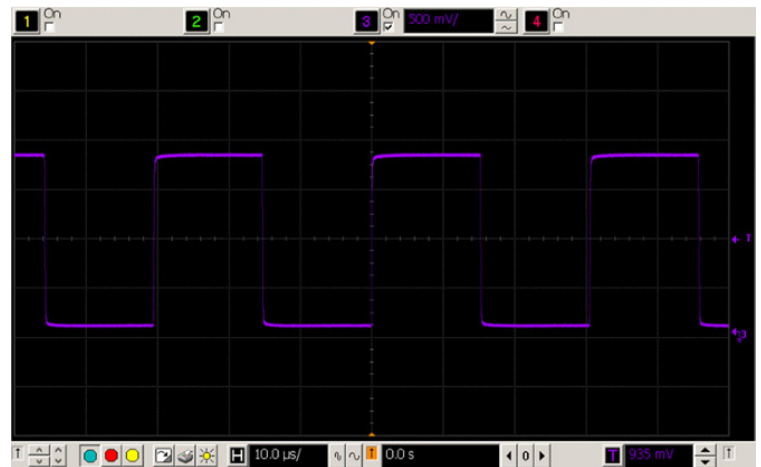
Start-up and Steady-State Current Profile



Frequency Stability Over Temperature



LVC MOS Output Waveform  
(MT-9560AE-JA-DCC-32K768, 10 pF Load)



## Calculating Load Current

### No Load Supply Current

When calculating no-load power for the MT-9560A, the core and output driver components need to be added. Since the output voltage swing can be programmed to minimize load current, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) =  $I_{dd}$  Core +  $I_{dd}$  Output Driver

#### Example 1: Full-swing LVC MOS

- $V_{dd} = 1.8\text{V}$
- $I_{dd}$  Core = 990nA (typ)
- $V_{outpp} = 1.8\text{V}$
- $I_{dd}$  Output Driver:  $(C_{driver})(V_{out})(F_{out}) = (3.5\text{pF})(1.8\text{V})(32768\text{Hz}) = 206\text{nA}$

Supply Current = 990nA + 206nA = 1.2μA

### Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below.

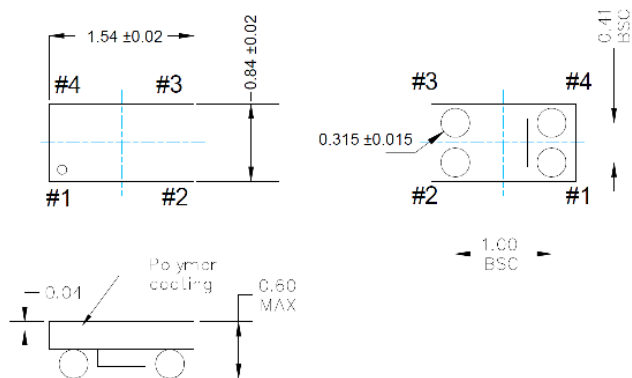
Total Current =  $I_{dd}$  Core +  $I_{dd}$  Output Driver + Load Current

#### Example 1: Full-swing LVC MOS

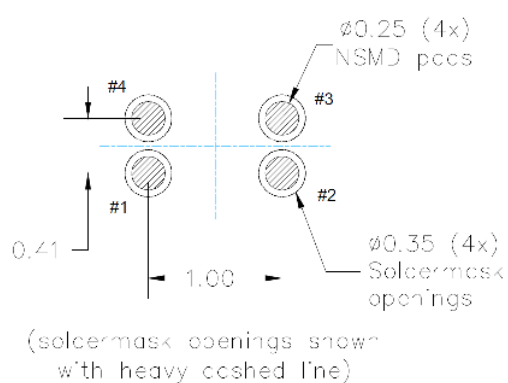
- $V_{dd} = 1.8\text{V}$
- $I_{dd}$  Core = 990nA
- Load Capacitance = 10pF
- $I_{dd}$  Output Driver:  $(C_{driver})(V_{out})(F_{out}) = (3.5\text{pF})(1.8\text{V})(32768\text{Hz}) = 206\text{nA}$
- Load Current:  $(10\text{pF})(1.8\text{V})(32768\text{Hz}) = 590\text{nA}$
- Total Current = 990nA + 206nA + 590nA = 1.79μA

# Packaging Options

## Package Outline & Dimensions (Unit: mm)



## Recommended Land Pattern (Unit: mm)



### Notes:

- Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device

# Ordering Information

## MT-9560A E - J A - D C C - 32K768

Family  
MT-9560A

Temp Range  
T: 0 to 70°C  
E: -40 to 85°C

Package Size  
J: 1.5 mm x 0.8 mm CSP

Stability  
A: ±5ppm  
B: ±10ppm  
E: ±20ppm

Output Clock Frequency (kHz)  
32.768 kHz

DC-coupled Output  $V_{OL}$  or AC Swing  
C: rail-to-rail LVCMOS

DC-coupled Output  $V_{OH}$   
C: rail-to-rail LVCMOS

AC- or DC-coupled  
D: DC-coupled Signal Path or  
Rail-to-Rail LVCMOS

## Revision History

Revision	Change Summary	Date
1.0	Product Release	August 2014
1.1	Removed Preliminary Designation	December 2014
1.2	Removed NanoDrive Capability	February 2015
1.3	Added Stabilities B and E	June 2015

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