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Vectron
a Knowles company

MOUNT HOLLY SPRINGS, PA 17065

Specification, Hybrid TCXO

Hi-Rel Standard

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UNSPECIFIED TOLERANCES: N/A

1. SCOPE

1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid TCXOs produced by Vectron International. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.

1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within DOC200103 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military, Ruggedized COTS or Commercial environments.

2. APPLICABLE DOCUMENTS

2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Standards

MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

Vectron International

QSP-90100	Quality Systems Manual, Vectron International
DOC007131	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification
QSP-91502	Procedure for Electrostatic Discharge Precautions

3. GENERAL REQUIREMENTS

3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 3, Class 2 of MIL-PRF-55310. Devices carry a Class 1C ESDS classification per MIL-PRF-38534 and are marked with a single equilateral triangle at pin 1 per MIL-PRF-55310.

3.2 Item Identification. External packaging choices are either metal flatpacks or DDIP with either Sinewave or CMOS logic output. Unique Model Number Series' are utilized to identify device package configurations and output waveform as listed in Table 1.

3.3 Absolute Maximum Ratings.

a. Supply Voltage Range (V_{CC}):	-0.5Vdc to +7.0Vdc (+5V CMOS) -0.5Vdc to +5.0Vdc (+3.3V CMOS) Contact factory for sinewave output
b. Storage Temperature Range (T_{STG}):	-65°C to +125°C
c. Junction Temperature (T_J):	+150C
d. Lead Temperature (soldering, 10 seconds):	+300°C

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. All designs utilize a 4-point crystal mount. For radiation characteristics, see paragraph 4.1.3. For all Class S and Class B products, components meet the Element Evaluation requirements of MIL-PRF-55310, Appendix B. If Design Pedigree Code "E" is chosen, Enhanced Element Evaluation per Appendix A herein will be performed.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without written approval from the procuring activity.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three minute duration in each of three mutually perpendicular directions)
c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.
b. Zinc chromate as a finish.
c. Cadmium, zinc, or pure tin external or internal to the device.
d. Plastic encapsulated semiconductor devices.
e. Ultrasonically cleaned electronic parts.
f. Heterojunction Bipolar Transistor (HBT) technology.

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on levels E and R per paragraph 7.1 to further verify lot pedigree. Traceability of all components and production lots are in accordance with MIL-PRF-38534, as a minimum. Tabulated records are provided as a part of the deliverable data package. Devices are handled in accordance with Vectron document QSP-91502 (Procedure for Electrostatic Discharge Precautions).

3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 derived system of QSP-90100.

3.4.5 Test. The Screening test matrix of Table 4 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310.

3.4.7 Ruggedized COTS Design Implementation. Design Pedigree "D" devices (see ¶ 5.2) use the same robust designs as the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in paragraphs 3.4.3 and 4.1.

4. DETAIL REQUIREMENTS

4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. Premium Q swept quartz is standard for all Class S level products because of its superior radiation tolerance. For Class B level products, swept quartz is optional, as required by the customer. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal evaluation program.

4.1.2 Passive Components. Passive components will have the same pedigree as the die specified in paragraph 7.1. Where possible, for Design Pedigrees 'E' & 'R', Established Reliability (ER) failure level R and S passive components are employed. Otherwise, all components comply with the Element Evaluation requirements of MIL-PRF-38534 or Enhanced Element Evaluation as specified in Appendix A herein. When used, inductors may be open construction and may use up to 47 gauge wire.

4.1.3 Class S Microcircuits. Microcircuits are procured from wafer lots that have passed MIL-PRF-38534 Class K Lot Acceptance Tests for Class S devices. Although radiation testing is not performed at the oscillator level, Design Pedigree Codes E and R versions of this TCXO are acceptable for use in environments of up to 100krad (Si) total dose as a result of wafer lot specific RLAT or by analysis of the individual components. Sinewave devices are assembled with all bipolar semiconductors. ACMOS devices are assembled with all bipolar semiconductors with the exception of the ACMOS chip used to provide the CMOS output. An ACMOS die from a radiation tested and certified wafer lot will be provided for all Class S versions of this TCXO. This microcircuit is certified for 100krads (Si) total ionizing dose (TID), RHA level R (2X minimum margin). NSC, as the 54ACT designer, rates the SET LET at > 40MeV and SEL at >120MeV for the FACT™ family (AN-932). Vectron has conducted additional SEE testing in 2008 to verify this performance since our lot wafer testing does not include these parameters and determinations.
A copy of the parts list and materials can be provided for customer review upon request.

4.1.3.1 Class B Microcircuits. When specified, microcircuits assembled into Pedigree Codes B and C devices (¶ 5.2a) are procured from wafer lots that have passed MIL-PRF-55310 element evaluations for Class B devices.

4.1.4 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are evaluated in accordance with the requirements of MIL-PRF-38534 as applicable.

4.1.5 Traceability and Homogeneity. All design pedigrees except option D have active device lots that are homogenous and traceable to the manufacturer's individual wafer. Swept Quartz Crystals are traceable to the quartz bar and the processing details of the autoclave lot, as applicable. All other elements and materials are traceable to their manufacturing lots. Manufacturing lot and date code information shall be recorded, by TCXO serial number, of every component and all materials used in the manufacture of that TCXO. All semiconductors used in the manufacture of a given production lot of TCXOs shall be from the same wafer and have the same manufacturing lot date code. A production lot, as defined by Vectron, is all oscillators that have been kitted and assembled as a single group. After the initial kitting and assembly, this production lot may be divided into multiple sublots to facilitate alignment and test capacity and may be sealed at multiple times within a 13 week window.

4.2 Mechanical.

4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure.

4.2.2 Thermal Characteristics. Because these TCXOs are multichip hybrid designs, the actual θ_{jc} to any one given semiconductor die will vary, but the combined average for all active devices results in a θ_{jc} of approximately 40°C/W. The typical die temperature rise at any one given semiconductor is 2°C to 4°C. With the oscillator operating at +125°C, the average junction temperature is approximately +129°C and under no circumstance will it ever exceed the maximum manufacturer's rated junction temperature.

4.3 Electrical.

4.3.1 Input Power. CMOS devices are designed for 3.3 ±5% or 5.0 volt ±5% DC operation. Sinewave devices are designed for 3.3, 5.0, 12.0 or 15.0 volt dc operation with ±5% tolerance.

4.3.2 Temperature Range. Operating range is IAW the chosen temperature stability code.

4.3.3 Frequency Tolerance. Temperature stability includes initial accuracy at +25°C (with EFC), load ±10% and supply ±5%.

4.3.4 All devices include an External Frequency Control (EFC) pin for the purpose of externally setting each TCXO to its nominal frequency. The EFC shall be accomplished by connecting a resistor or trimmer potentiometer from that Pin to GND. The EFC resistance adjustment range is 0Ω or GND to 20KΩ max with Nominal frequency typically occurring in the 5KΩ to 10KΩ range. Customers will be furnished with the applicable EFC resistor value that can be used to set each individual device within ±0.2 ppm of nominal frequency at time of shipment.

4.3.5 Frequency Aging. Aging limits, when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1 ppm for the first year and ±5 ppm for 15 years for oscillators that use crystals in the 10 MHz to 75 MHz range. For oscillators that use crystals greater than 75 MHz, the aging shall not exceed ±2 ppm for the first year and ±10 ppm for 15 years.

4.3.5.1 Frequency Aging Duration Option. By customer request, the Aging test may be terminated after 15 days if the aging projection is less than the specified aging limit. This is a common method of expediting 30-day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. Vectron's automated aging systems acquire data every four hours, compared to the minimum MIL-PRF-55310 requirement of once every 72 hours. This makes an extensive amount of data available to perform very accurate aging projections. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit then they would continue to the full 30-day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.6 Operating Characteristics. See Tables 2 and 3. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310. Start-up time is 10 msec typical and 30 msec maximum.

4.3.7 Output Load. Standard Sinewave (50 ohms) and CMOS (10kΩ, 15pF) test loads are in accordance with MIL-PRF-55310.

4.3.8 Phase Noise. Contact factory for typical performance. If custom and/or guaranteed performance is required, Vectron can assign a custom part number.

5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 16th character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A Testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

(K) Modified MIL-PRF-38534 Class K Screening, Group A QCI and 30-day aging
(S) MIL-PRF-55310 Class S Screening, Groups A & B QCI
(C) Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
(B) MIL-PRF-55310 Class B Screening, Groups A & B QCI
(X) Engineering Model (EM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection and test options that can be added by purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):
   (E) Class S components, Enhanced Element Evaluation, Swept Quartz
   (R) Class S components, Swept Quartz
   (B) Class B components, Swept Quartz
   (C) Class B components, Non-Swept Quartz
   (D) COTS components, Non-Swept Quartz
b. Input Voltage as the 15th character
c. Frequency-Temperature Slew Test
d. Radiographic Inspection
e. Group C Inspection: MIL-PRF-55310 (requires 8 destruct specimens)
f. Group C Inspection: MIL-PRF-38534, Table C-Xc, Periodic Inspection (requires 10 destruct specimens – 5 pc. [SG 1(5/0), SG 3(3/0)], 5 pc. SG 2 (5/0). Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Condition C.
g. Internal Water-Vapor Content (RGA) samples and test performance
h. MTBF Reliability Calculations
i. Worst Case/Derating Analysis
j. Deliverable Process Identification Documentation (PID)
k. Customer Source Inspection (pre-cap / final) [Note: Model numbers 2105, 2205, 2115 and 2215 require two pre-cap inspections.]
l. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Vectron DOC203982.
m. Qualification: In accordance with MIL-PRF-55310, Table IV (requires 11 destruct specimens).
n. Qualification: In accordance with EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)
o. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum)
p. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping.

5.2.1 NASA EEE-INST-002. A combination of design pedigrees E or R along with Screening option S and Group C Inspection in accordance with MIL-PRF-55310, meet the requirements of Level 1 device reliability. A combination of design pedigrees B or C along with screening option C and Group C Inspection in accordance with MIL-PRF-55310, meet the requirements of Level 2 device reliability.

5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.4 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices:

a. Completed assembly and screening lot travelers, including rework history and Certificate of Conformance.

b. Electrical test variables data, identified by unique serial number.

c. Frequency-Temperature Slew plots, Radiographic data, Group C data and RGA data as required by purchase order.

d. Traceability, component LAT, enclosure LAT and RLAT (if specifically requested on the purchase order).

5.5 Discrepant Material. All MRB authority resides with the procuring activity.

5.6 Failure Analysis. Any catastrophic failure (no output, no input current) at Post Burn-In or after will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

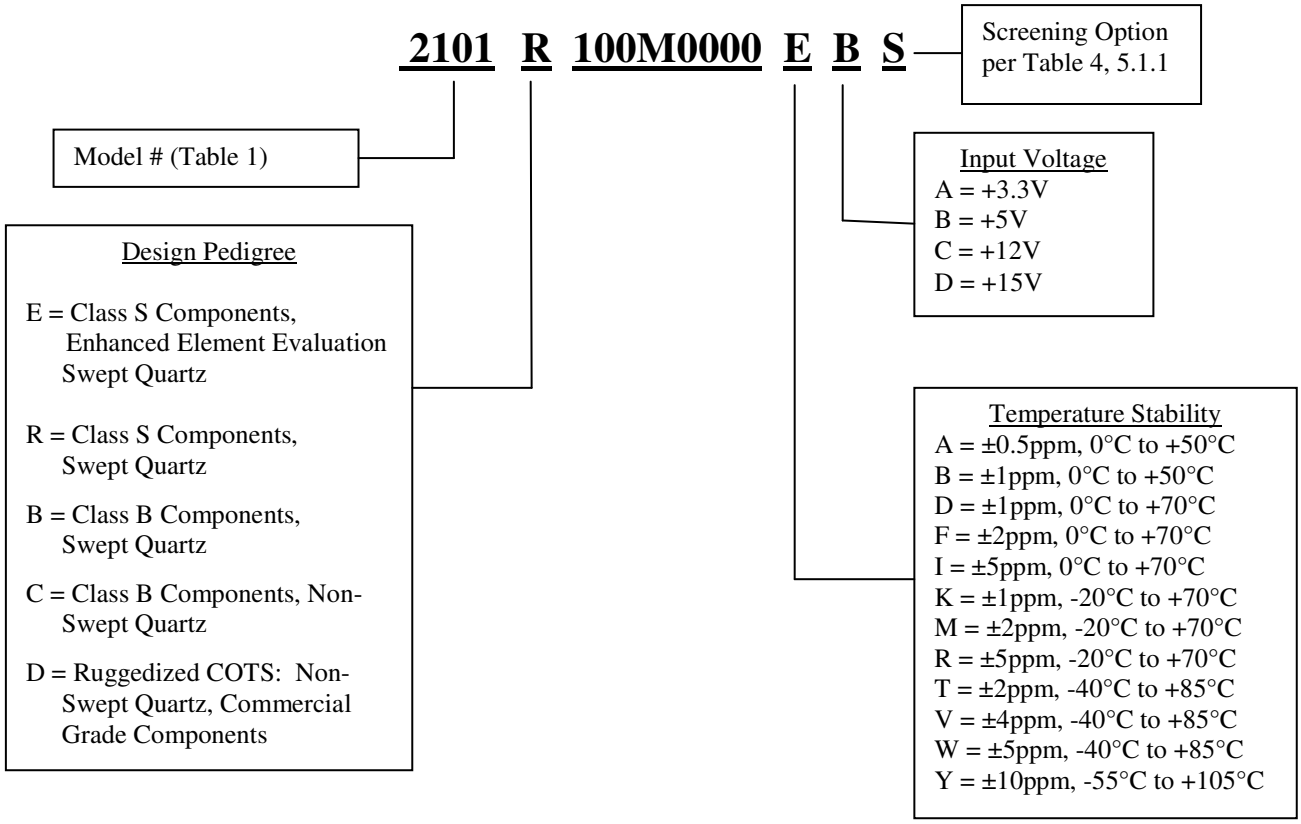
6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling, ESD and transit damage during shipping.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 16 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (¶ 5.2a and b), are included within the device part number.

The Part Number breakdown is described as:



7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.

7.1.2 Design Pedigree. Class S designs correspond to letters "E" and "R" and are described in paragraph 5.2a. Class B variants correspond to either letter "B" or "C" and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, correspond to letter "D".

7.1.2.1 Input Voltage. Voltage is the 15th character. Voltage availability is dependant on platform.

7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

7.1.4 Screening Options. The 16th character is the Screening Option selected from Table 4.

7.2 Optional Design, Test and Data Parameters. Test and documentation requirements above that of the standard high reliability model shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru p).

HI-REL STANDARD MODEL #	PACKAGE	OUTPUT	PIN I/O 1/				MECHANICAL OUTLINE
			Vcc	Out	Gnd/Case	EFC	
2101	24 Pin DDIP	CMOS	24	13	12	1	FIGURE 1
2102	32 Lead Flatpack	CMOS	11, 13	12	5	4	FIGURE 2
2103	24 Lead Flatpack	CMOS	24	13	12	1	FIGURE 3
2104	14 Lead Flatpack	CMOS	2	13	1, 3, 7, 12, 14	6	FIGURE 4
2105	14 Lead Flatpack	CMOS	14	8	2, 7, 9, 13	1	FIGURE 5
2202 2/	32 Lead Flatpack	CMOS	11, 13	12	5	4	FIGURE 6
2203 2/	24 Lead Flatpack	CMOS	24	13	12	1	FIGURE 7
2204 2/	14 Lead Flatpack	CMOS	2	13	1, 3, 7, 12, 14	6	FIGURE 8
2205 2/	14 Lead Flatpack	CMOS	14	8	2, 7, 9, 13	1	FIGURE 9
2111	24 Pin DDIP	Sine	24	13	12	1	FIGURE 1
2112	32 Lead Flatpack	Sine	11, 13	12	5	4	FIGURE 2
2113	24 Lead Flatpack	Sine	24	13	12	1	FIGURE 3
2114	14 Lead Flatpack	Sine	2	13	1, 3, 7, 12, 14	6	FIGURE 4
2115	14 Lead Flatpack	Sine	14	8	2, 7, 9, 13	1	FIGURE 5
2212 2/	32 Lead Flatpack	Sine	11, 13	12	5	4	FIGURE 6
2213 2/	24 Lead Flatpack	Sine	24	13	12	1	FIGURE 7
2214 2/	14 Lead Flatpack	Sine	2	13	1, 3, 7, 12, 14	6	FIGURE 8
2215 2/	14 Lead Flatpack	Sine	14	8	2, 7, 9, 13	1	FIGURE 9

1/. All unassigned pins have no internal connections or ties and may be externally connected to GND by the customer.

2/. Models 2202 through 2205 and 2212 through 2215 represent lead formed versions.

TABLE 1 - Item Identification and Package Outline

Model Number	Package	Typical Weight (Grams)
2101, 2111	24 Pin DDIP	21
2102, 2202, 2112, 2212	32 Lead Flatpack	10
2103, 2203, 2113, 2213	24 Lead Flatpack	16
2104, 2204, 2114, 2214	14 Lead Flatpack	19
2105, 2205, 2115, 2215	14 Lead Flatpack	8

TABLE 1A – Typical Weight

Models 2101, 2102, 2103, 2104, 2105, 2202, 2203, 2204, 2205						
Supply Voltage Options1/: +3.3V or +5V						
Frequency Range (MHz)	Max Current (mA)		Max t_r/t_f (ns) 2/	Duty Cycle (%) 2/	Max CMOS Load (pF)	
	5.25V	3.465V			5.25V	3.465V
0.300 - 100	50	35	5	40 to 60	50	35

1/. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310.
2/. Tested with 15pF.

TABLE 2 - Electrical Performance Characteristics

Model 2111						
Supply Voltage Options: +3.3V, +5V, +12V or +15V						
Frequency Range (MHz)	Max Current (mA)		Min Power Out (dBm)		Harmonics/ Subharmonics (>75MHz) (dBc)	Spurious (dBc)
	3.3V/5V	12V/15V	3.3V/5V	12V/15V		
10 - 225	20	35	+3	+7	< -20	< -70

TABLE 2A - Electrical Performance Characteristics

Models 2112, 2114, 2115, 2212, 2214, 2215							
Supply Voltage Options: +3.3V, +5V, +12V or +15V							
Frequency Range (MHz)	Max Current (mA)		Min Power Out (dBm)			Harmonics/ Subharmonics (>75MHz) (dBc)	Spurious (dBc)
	3.3V/5V	12V/15V	3.3V	5V	12V/15V		
10 - 150	20	35	0	+3	+7	< -20	< -70

TABLE 2B - Electrical Performance Characteristics

Model 2113, 2213						
Supply Voltage Options: +12V or +15V						
Frequency Range (MHz)	Max Current (mA)		Min Power Out (dBm)		Harmonics/ Subharmonics (>75MHz) (dBc)	Spurious (dBc)
	12V	15V	12V	15V		
10 – 500	25	35	+5	+7	< -20	< -70

TABLE 2C - Electrical Performance Characteristics

OPERATION LISTING	REQUIREMENTS AND CONDITIONS	VECTRON TEST PROCEDURE
Input Current (no load)	MIL-PRF-55310, Para 4.8.5.1	GR-51681
Initial Accuracy @ Ref. Temp.	MIL-PRF-55310, Para 4.8.6	GR-51596
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3	GR-51597
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22	GR-51599
Duty Cycle	MIL-PRF-55310, Para 4.8.23	GR-51601
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4	GR-37269
Initial Freq. – Temp. Accuracy	MIL-PRF-55310, Para 4.8.10.1	DOC005199
Freq. – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14	DOC005199
Start-up Time (fast/slow start)	MIL-PRF-55310, Para 4.8.29	GR-61352

TABLE 3 - Electrical Test Parameters

SCREENING & TESTING OPTIONS					
Option Code	**K**	**S**	**C**	**B**	**X**
Screening (By Class Similarity)	Mil-PRF-38534 Class 'K'	Mil-PRF-55310 Class 'S'	Mil-PRF-55310 Class 'B' modified	Mil-PRF-55310 Class 'B'	Engineering Model (EM)
Non-Destruct Wire Bond Pull	100%	100%	N/A	N/A	N/A
Internal Visual	M883, Method 2017 for Class 'K'	M883, Method 2017 for Class 'K'	M883, Method 2017 for Class 'H'	M883, Method 2017 for Class 'H'	M883, Method 2017 for Class 'H'
Stabilization Bake	48 hrs min @ +150°C	48 hrs min @ +150°C	48 hrs min @ +150°C	48 hrs min @ +150°C	24 hrs min @ +150°C
Thermal Shock	M883, Method 1011, TC 'A'	M883, Method 1011, TC 'A'	N/A	N/A	N/A
Temperature Cycling	M883, Method 1010, TC 'B'	M883, Method 1010, TC 'B'	M883, Method 1010, TC 'B'	M883, Method 1010, TC 'B'	N/A
Constant Acceleration	M883, Method 2001, TC 'A' (5000 g, Y1 Axis only)	M883, Method 2001, TC 'A' (5000 g, Y1 Axis only)	M883, Method 2001, TC 'A' (5000 g, Y1 Axis only)	M883, Method 2001, TC 'A' (5000 g, Y1 Axis only)	N/A
PIND	M883, Method 2020, TC 'B'	M883, Method 2020, TC 'B'	M883, Method 2020, TC 'B'	N/A	N/A
Electrical Test Frequency, Output levels, Input Current	@ +25°C only	@ +25°C only	@ +25°C only	@ +25°C only	@ +25°C only
1st Burn-In (Powered with load)	+125°C for 160 hours	+125°C for 240 hours	+125°C for 160 hours	+125°C for 160 hours	N/A
Electrical Test Frequency, Output levels, Input Current	@ +25°C & Temp Extremes	@ +25°C & Temp Extremes	@ +25°C & Temp Extremes	@ +25°C & Temp Extremes	N/A
2nd Burn-In (Powered with load)	+125°C for 160 hours	N/A	N/A	N/A	N/A
Electrical Test Frequency, Output levels, Input Current	@ +25°C & Temp Extremes	N/A	N/A	N/A	N/A
PDA	2% applies to Input Current @ +25°C Post 2ND Burn-in Electrical Test	2% applies to Input Current @ +25°C	10% applies to Input Current @ +25°C	10% applies to Input Current @ +25°C	N/A
Radiographic	M883, Method 2012	M883, Method 2012	M883, Method 2012	N/A	N/A
Seal Test (fine & gross)	100%	100%	100%	100%	100%
Group 'A' Inspection	100%	100%	Sample per Mil-PRF-55310	Sample per Mil-PRF-55310	N/A
Group 'B' Inspection (30 day Aging @ +70°C)	100%	100%	Sample per Mil-PRF-55310	Sample per Mil-PRF-55310	N/A

TABLE 4 - Screening & Test Matrix

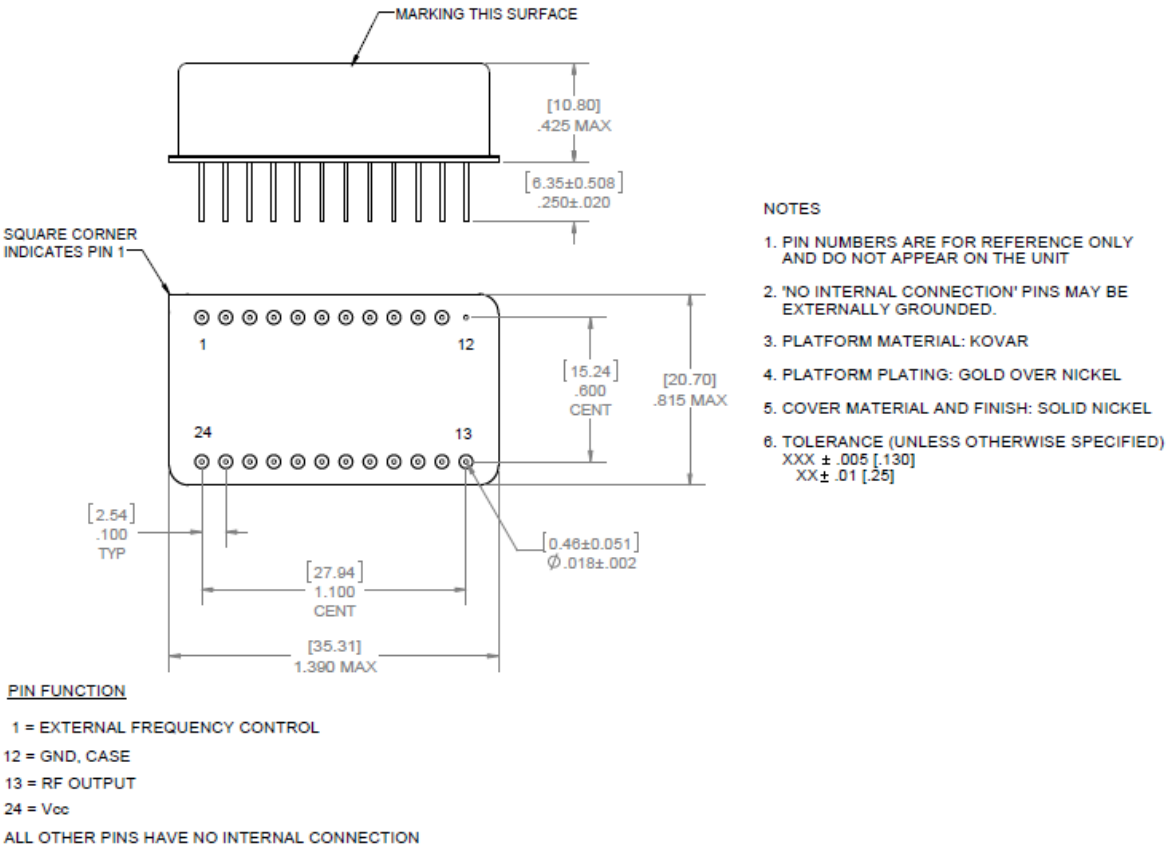


FIGURE 1
Models 2101 & 2111 Package Outline

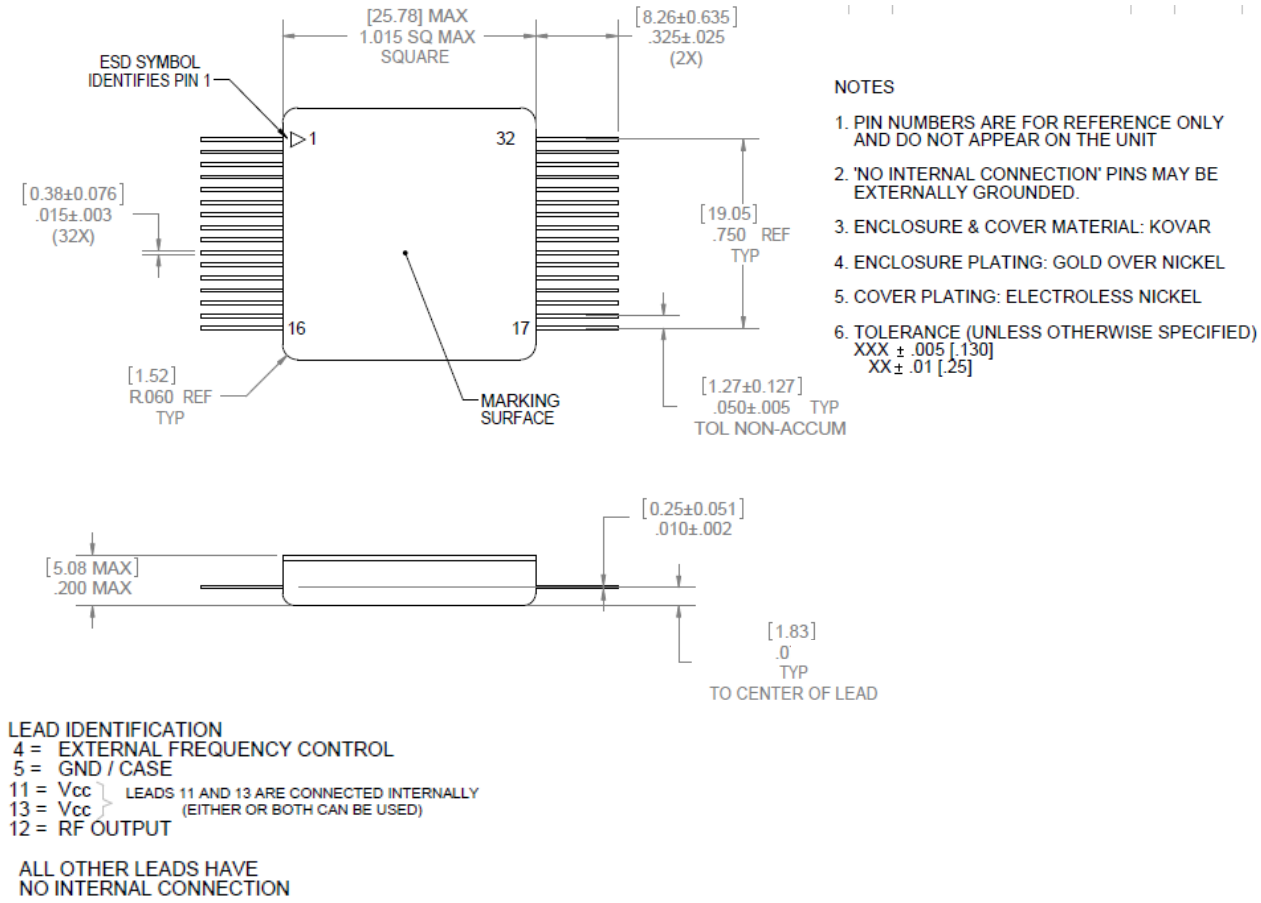


FIGURE 2
Models 2102 & 2112 Package Outline

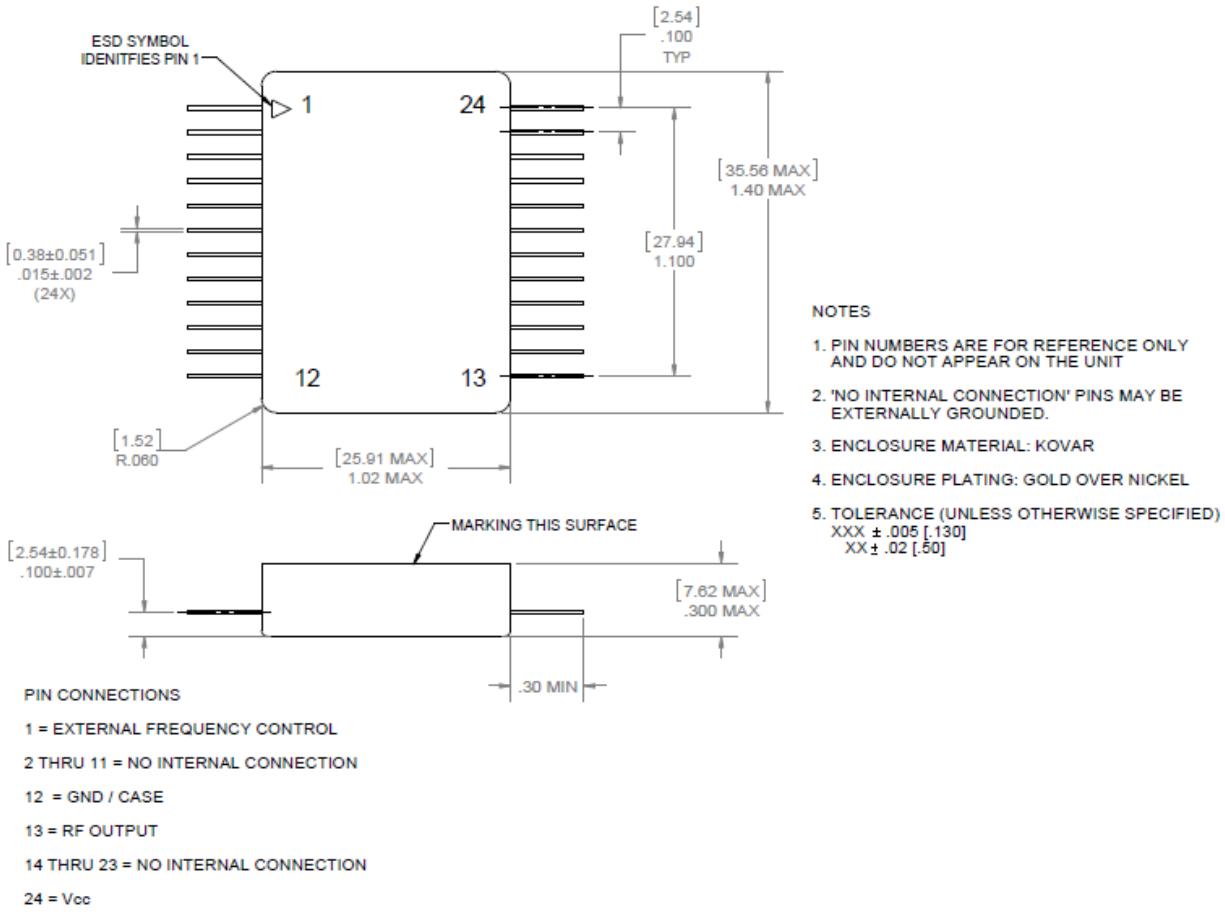


FIGURE 3
Models 2103 & 2113 Package Outline

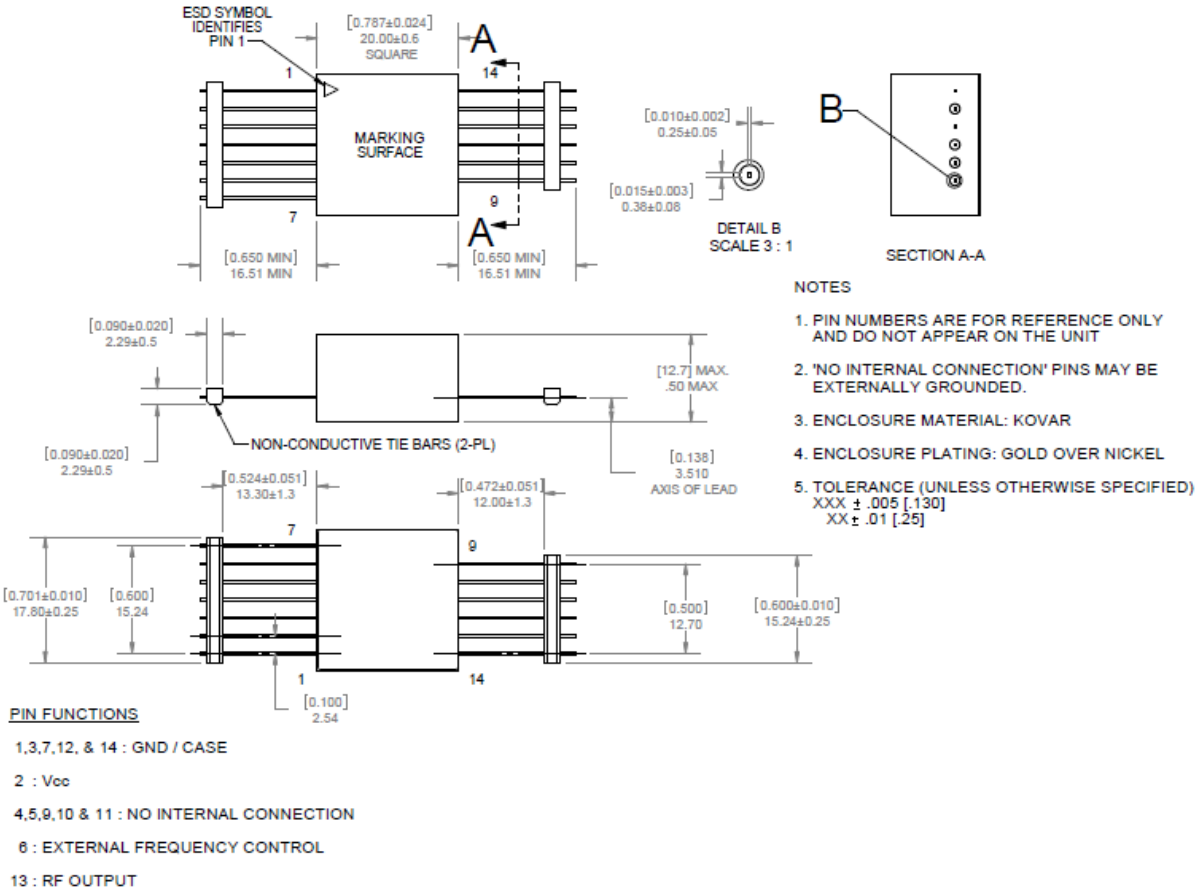
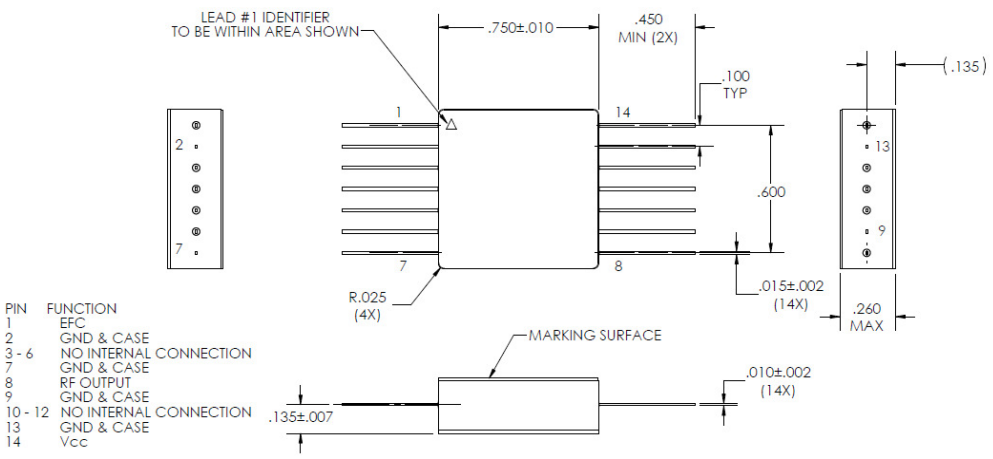


FIGURE 4
Models 2104 & 2114 Package Outline



PIN	FUNCTION
1	EFC
2	GND & CASE
3 - 6	NO INTERNAL CONNECTION
7	GND & CASE
8	RF OUTPUT
9	GND & CASE
10 - 12	NO INTERNAL CONNECTION
13	GND & CASE
14	Vcc

NOTES:

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
2. " NO INTERNAL CONNECTION" PINS MAY EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. TOLERANCE (UNLESS OTHERWISE SPECIFIED)
   XXX ±.005
   XX ±.02

FIGURE 5
Model 2105 and 2115 Package Outline

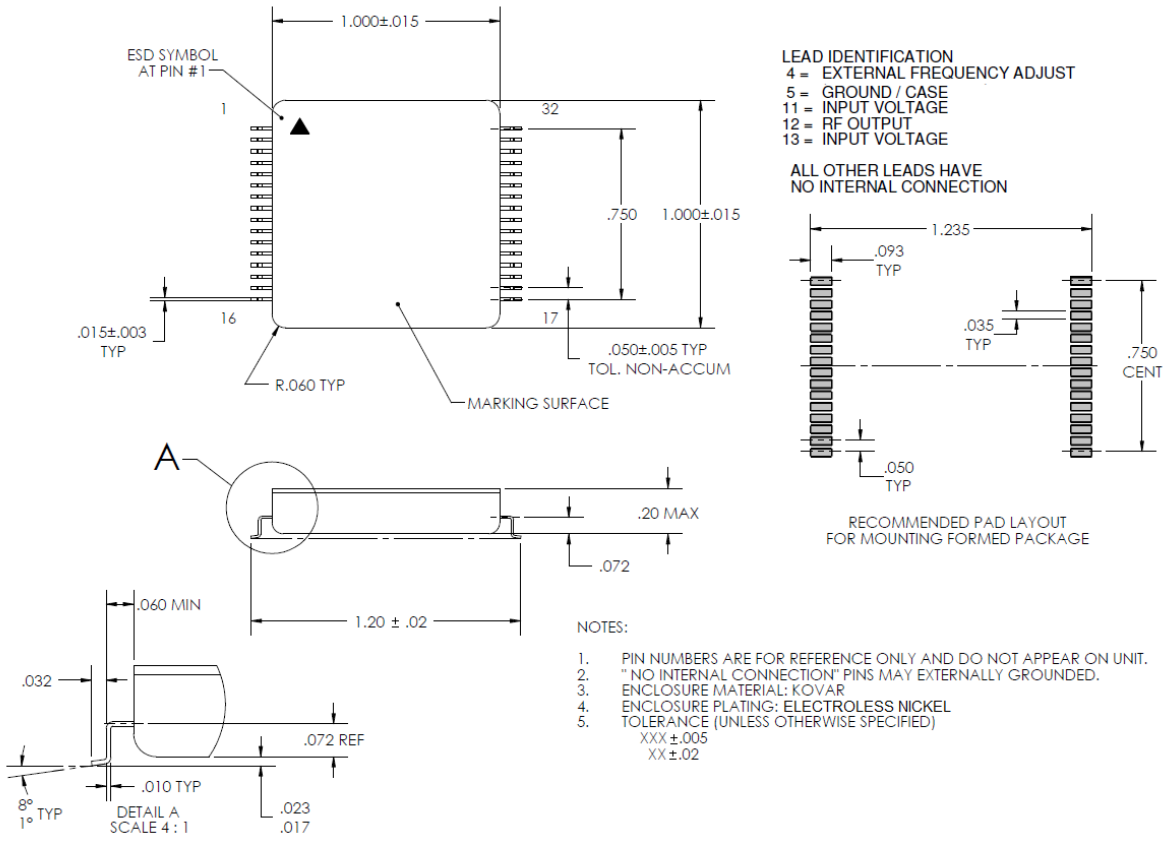


FIGURE 6
Models 2202 and 2212 Package Outline and Land Pattern

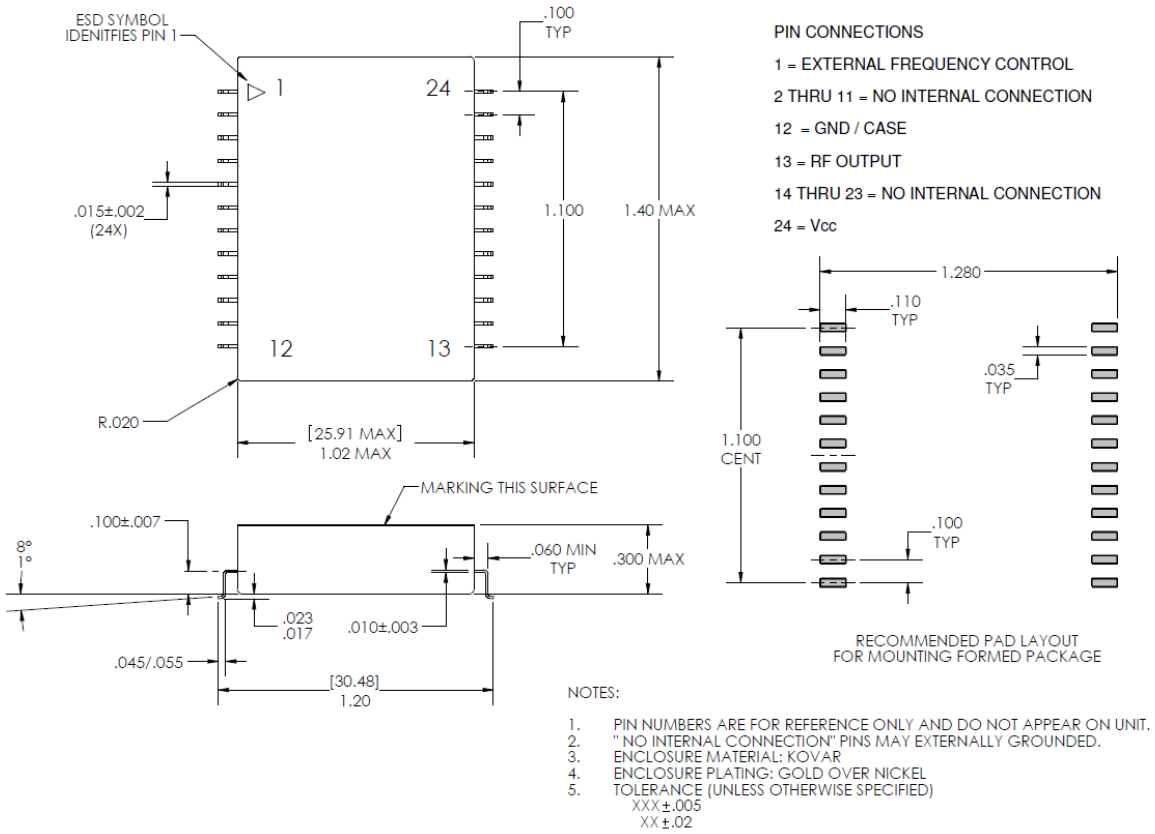
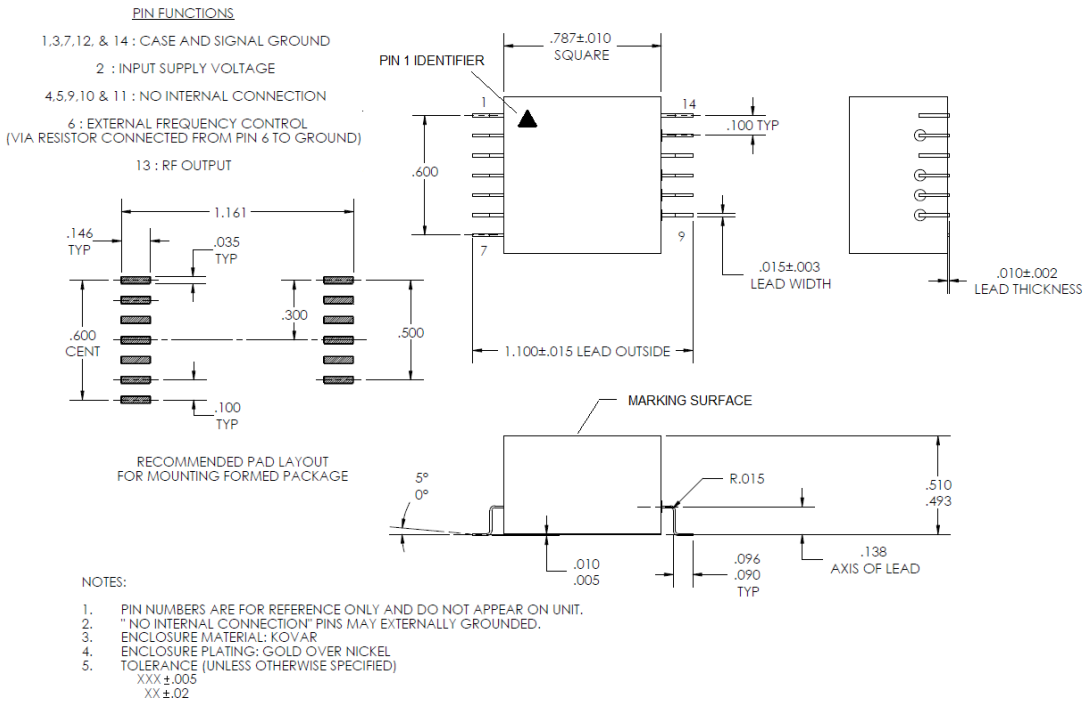


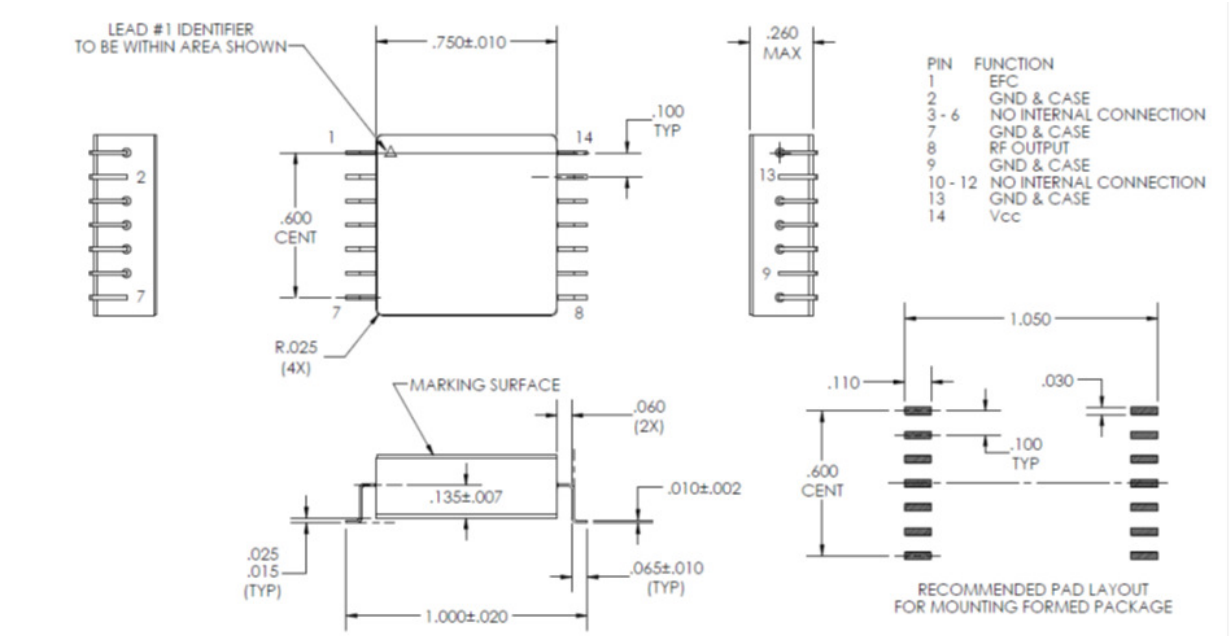
FIGURE 7
Models 2203 and 2213 Package Outline and Land Pattern



NOTES:

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
2. " NO INTERNAL CONNECTION" PINS MAY EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. TOLERANCE (UNLESS OTHERWISE SPECIFIED)
   XXX ±.005
   XX ±.02

FIGURE 8
Models 2204 and 2214 Package Outline and Land Pattern



NOTES:

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
2. " NO INTERNAL CONNECTION" PINS MAY EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. TOLERANCE (UNLESS OTHERWISE SPECIFIED)
   XXX ±.005
   XX ±.02

FIGURE 9
Model 2205 and 2215 Package Outline and Land Pattern

Appendix A

ENHANCED ELEMENT EVALUATION

MICROCIRCUIT ENHANCED ELEMENT EVALUATION

Subgroup	Class K	Test	Mil-STD-883 Method	Mil-STD-883 Condition	Quantity (accept number)	Mil-PRF-38534 Reference Paragraph
1	X	Element Electrical A. May perform at wafer level B. All failures shall be removed from the lot C. Perform at room ambient			100%	C.3.3.1
2	X	Element Visual	2010		100%	C.3.3.2
3	X	Internal Visual	2010		10(0) or 22(0) (See Notes 1 & 2)	C.3.3.3 C.3.3.4.2
4	X	Temperature Cycling	1010	C	10(0) 22(0) (See Notes 1 & 2)	C.3.3.3
	X	Mechanical Shock or Constant Acceleration	2002 2001	B, Y1 direction 3,000 G, Y1 direction		
	X	Interim Electrical				C.3.3.4.3
	X	Burn-In	1015	240 hours minimum at +125°C		
	X	Post Burn-In Electrical				C.3.3.4.3
	X	Steady State Life	1005			
	X	Final Electrical				C.3.3.4.3
5	X	Wire Bond Evaluation	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	X	SEM	2018		See method 2018 & Note 2	C.3.3.6

NOTES:

1. Subgroups 3, 4, & 5 shall be performed on a sample of 10 die if the wafer lot is from a QPL/QML line. If the die are from commercial wafer lots, then the sample size shall be 22 die. Die from QPL/QML wafers not meeting the QPL/QML requirements and downgraded to commercial grade shall not be used.
2. Subgroups 3, 4 & 5 shall be performed in the order listed in Table 1. Subgroup 6 may be performed at any time.

SEMICONDUCTOR ENHANCED ELEMENT EVALUATION

Subgroup	Class K	Test	Mil-STD-750 Method	Mil-STD-750 Condition	Quantity (accept number)	Mil-PRF-38534 Reference Paragraph
1	X	Element Electrical A. May perform at wafer level B. All failures shall be removed from the lot		Perform at room ambient	100%	C.3.3.1
2	X	Element Visual	2069, 2070, 2072, 2073		100%	C.3.3.2
3	X	Internal Visual	2069, 2070, 2072, 2073, 2074		10(0) or 22(0) (Notes 1 & 2)	C.3.3.3 C.3.3.4.2
4	X	Temperature Cycling	1051	C	10(0) 22(0) (See Notes 1 & 2)	C.3.3.3
	X	Surge Current (when applicable)	4066	A or B as specified		
	X	Constant Acceleration	2006 2001	Y1 direction 20,000 G / 10,000 G for Pd ≥ 10W		
	X	Interim Electrical				C.3.3.4.3
	X	High Temperature Reverse Bias (HTRB)	1039 1042 1038	A B A		
	X	Interim Electrical & Delta		Complete Within 16 hrs of HTRB completion		
	X	Burn-In 240 hours	1039, 1042 1038 1040	B, A B		
	X	Post Burn-In Electrical				C.3.3.4.3
	X	Steady State Life 1000 hours or equivalent per MIL-PRF-19500	1026 1037 1042 1048			
	X	Final Electrical				C.3.3.4.3
5	X	Wire Bond Evaluation	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	X	SEM	2018 2077		See method 2018 or 2077 & Note 2	C.3.3.6

NOTES:

1. Subgroups 3, 4, & 5 shall be performed on a sample of 10 die if the wafer lot is from a QPL/QML line. If the die are from commercial wafer lots, then the sample size shall be 22 die. Die from QPL/QML wafers not meeting the QPL/QML requirements and downgraded to commercial grade shall not be used.
2. Subgroups 3, 4 & 5 shall be performed in the order listed in Table 1. Subgroup 6 may be performed at any time.

PASSIVE COMPONENTS ENHANCED ELEMENT EVALUATION

Part Type	Test	Requirements Paragraph	Sample Size	Allowable Rejects
Ceramic capacitors (Production lot definition shall be per M55681 or M123 for chips, or M49470 T-level for stacks)				
M55681 FRL S or M123 (chips)	N/A	N/A	N/A	N/A
DSCC Dwg COTS (chips)	Ultrasonic scan or CSAM	M123	100%	N/A
	Group A	M123	M123	M123
	Group B, Subgroups 1 & 2	M123	M123	M123
T-level M49470 (stacked)	N/A	N/A	N/A	N/A
General purpose M49470, DSCC dwg or COTS (stacked)	Ultrasonic scan or CSAM	M49470 for T-level	100%	N/A
	Group A	M49470 for T-level	M49470 for T-level	M49470 for T-level
	Group B, Subgroups 2, 4 & 5b	M49470 for T-level	M49470 for T-level	M49470 for T-level
Tantalum Chip Capacitors (Note: Stacking tantalum chips will require a repeat of the entire Group A in M55365 with minimum Weibull C and surge current option C. Production lot definition shall be per M55365.)				
M55365	Group A (Weibull C minimum with surge current option C)	M55365	M55365	M55365
DSCC Dwg, COTS	Group A (Weibull C minimum with surge current option C)	M55365	M55365	M55365
	Group C	M55365	M55365	M55365
Resistor Chips (Note: Gluing one resistor chip on top of another to change a design or save on real estate is not allowable without extensive design/process verification, long term testing, and hybrid re-qualification. Production lot definition shall be per M55342).				
M55342 FRL R or S	N/A	N/A	N/A	N/A
DSCC Dwg, COTS	Group A	M55342 for T-level	M55342 for T-level	M55342 for T-level
	Group B	M55342 for T-level	M55342 for T-level	M55342 for T-level
Inductors (See Paragraph 4.1.2)				
Magnetics, Closed Construction Leaded and Surface Mount (transformers, inductors, coils) (Note: Stacking magnetics shall be qualified and the effects of the long term performance of the hybrids verified. When stacking magnetics, a repeat of the thermal cycling plus electrical measurements as specified in Group A of Mil-Std-981. Design, workmanship and materials/processes shall conform to MIL-STD-981 requirements). Magnetics, Open Construction are unencapsulated and unpotted self-leaded parts consisting of magnet wire wound around a magnetic core. These parts are fully visually inspectable. Open construction magnetics shall be subjected to 100% electrical measurements and visual inspection per Mil-Std-981.				
Custom closed magnetics	Group A	Mil-STD-981	Mil-STD-981	Mil-STD-981
	Group B	Mil-STD-981	Mil-STD-981	Mil-STD-981