REV	DESCRIPTION	DATE	PREP	APPD
C		11/13/20	HLW	HLW

MOUNT HOLLY SPRINGS, PA 17065

Specification, Hybrid TCXO

Hi-Rel Standard, LVDS Output

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CODE IDENT NO	SIZE	DWG. NO.	REV
00136	A	DOC207139	C

UNSPECIFIED TOLERANCES: N/A

1. SCOPE

1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid TCXOs produced by Vectron. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.

1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within DOC207139 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military, Ruggedized COTS or Commercial environments.

2. APPLICABLE DOCUMENTS

2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Standards

MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

Vectron

QSP-90100	Quality Systems Manual, Vectron
DOC011627	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification
QSP-91502	Procedure for Electrostatic Discharge Precautions
DOC208191	Enhanced Element Evaluation for Space Level Hybrid Oscillators

3. GENERAL REQUIREMENTS

3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 3, Class 2 of MIL-PRF-55310. Devices carry a Class 1C ESDS classification per MIL-PRF-38534 and are marked with a single equilateral triangle at pin 1 per MIL-PRF-55310.

3.2 Item Identification. Unique Model Number Series' are utilized to identify device package configurations as listed in Table 1.

3.3 Absolute Maximum Ratings.

a. Supply Voltage Range (V_{CC}):	-0.3Vdc to +4.0Vdc
b. Storage Temperature Range (T_{STG}):	-65°C to +125°C
c. Junction Temperature (T_J):	+150C
d. Lead Temperature (soldering, 10 seconds):	+300°C
e. Weight	25 grams

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. All designs utilize a 4-point crystal mount. For radiation characteristics, see paragraph 4.1.5. Section 4.0 details the component requirements for the various oscillator design pedigrees.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without written approval from the procuring activity.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three-minute duration in each of three mutually perpendicular directions)
c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.
b. Zinc chromate as a finish.
c. Cadmium, zinc, or pure tin external or internal to the device.
d. Plastic encapsulated semiconductor devices.
e. Ultrasonically cleaned electronic parts.
f. Heterojunction Bipolar Transistor (HBT) technology.

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on design pedigrees E and R per paragraph 7.1 to further verify lot pedigree. Devices are handled in accordance with Vectron document QSP-91502 (Procedure for Electrostatic Discharge Precautions). Element replacement will be as specified in MIL-PRF-38534, Rev L.

3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 and AS9100 derived system of QSP-90100.

3.4.5 Test. The Screening test matrix of Table 4 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310.

3.4.7 Ruggedized COTS Design Implementation. Design Pedigree “D” devices (see ¶ 5.2) use the same robust designs as the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in paragraphs 3.4.3 and 4.1.

4. DETAIL REQUIREMENTS

4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. Premium Q swept quartz is standard for all Design Pedigrees E, R and B because of its superior radiation tolerance. The manufacturer has a documented crystal evaluation program in accordance with MIL-PRF-55310.

4.1.2 Passive Components

4.1.2.1 For Design Pedigree E, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Enhanced Element Evaluation of DOC208191 which meets the requirements of Mil-PRF-38534 Revision L for Class K.

4.1.2.2 For Design Pedigree R, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Class K Element Evaluation of Mil-PRF-38534 Revision K for Class K.

4.1.2.3 For Design Pedigrees B and C, all passive elements shall comply with the Element Evaluation requirements of Mil-PRF-55310 Class B as a minimum.

4.1.2.4 For Design Pedigree D, the passive elements will be COTs level or higher.

4.1.3 Microcircuits (voltage regulators, LVDS devices, etc)

4.1.3.1 For Design Pedigree E, the LVDS microcircuit die is sourced in accordance with Standard Microcircuit Drawing 5962F9865107V9A, Class V (MIL-PRF-38535) qualified device. Other microcircuits shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191 and meet the requirements of Mil-PRF-38534 Revision L for Class K.

4.1.3.2 For Design Pedigree R, the LVDS microcircuit die is sourced in accordance with Standard Microcircuit Drawing 5962F9865107V9A, Class V (MIL-PRF-38535) qualified device. Other microcircuits shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K.

4.1.3.3 For Design Pedigrees B and C, microcircuits are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B as a minimum.

4.1.3.4 For Design Pedigree D, microcircuits can be COTs level or higher.

4.1.4 Semiconductors (transistors, diodes, etc)

4.1.4.1 For Design Pedigree E, the semiconductors shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191 and meet the requirements of Mil-PRF-38534 Revision L for Class K.

4.1.4.2 For Design Pedigree R, semiconductors shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K devices as a minimum.

4.1.4.3 For Design Pedigree B and C, semiconductors are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B devices as a minimum.

4.1.4.4 For Design Pedigree D, semiconductors can be COTs level or higher.

4.1.5 Radiation

Radiation testing is not performed at the oscillator level, however, Design Pedigrees E and R use microcircuits and semiconductors from wafer lots that have been evaluated up to 100krad (Si) total ionizing dose minimum.

In addition, the bipolar semiconductors are considered insensitive to Single Event Effects. The LVDS output buffer (5962F9865107V9A) is rated to SEL >135 MeV-cm^2/mg and SET/SEU to a threshold of 67 MeV-cm^2/mg. Varactor diodes are considered insensitive to total ionizing dose and single event effects.

4.1.6 Traceability and Homogeneity. All design pedigrees except option D have active device lots that are homogenous and traceable to the manufacturer's individual wafer. Swept Quartz crystals are traceable to the quartz bar and the processing details of the autoclave lot, as applicable. For design pedigrees E and R only, passive elements and materials are traceable to their manufacturing lots. Manufacturing lot and date code information shall be recorded, by TCXO serial number, of every component and all materials used in the manufacture of those TCXOs. A production lot, as defined by Vectron, is all oscillators that have been kitted and assembled as a single group. After the initial kitting and assembly, this production lot may be divided into multiple sublots to facilitate alignment and test capacity.

4.1.7 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are evaluated in accordance with the requirements of MIL-PRF-38534. Vectron will not perform Salt Spray testing as part of MIL-PRF-55310 Group C/Qualification. In accordance with MIL-PRF-55310, package evaluation results for salt atmosphere will be substituted for Salt Spray testing during MIL-PRF-55310 Group C/Qualification.

4.2 Mechanical.

4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure. Typical weight for all model numbers is 16 grams.

4.2.2 Thermal Characteristics. Because these TCXOs are multichip hybrid designs, the actual θ_{jc} to any one given semiconductor die will vary, but the combined average for all active devices results in a θ_{jc} of approximately 40°C/W. The typical die temperature rise at any one given

semiconductor is 2°C to 4°C. Under no circumstance will the junction temperature ever exceed the maximum manufacturer's rated junction temperature when operated within the maximum operating temperature range.

4.2.3 Lead Forming. When lead forming option is specified, the applicable leak test specified in screening will be performed after forming.

4.3 Electrical.

4.3.1 Supply Voltage. 3.3 ±5% Vdc operation.

4.3.2 Temperature Range. Operating range is IAW the chosen temperature stability code.

4.3.3 Frequency Tolerance. Temperature stability includes initial accuracy at +25°C (with EFC), load ±10% and supply ±5%.

4.3.4 All devices include an External Frequency Control (EFC) pin for the purpose of externally setting each TCXO to its nominal frequency. The EFC shall be accomplished by connecting a resistor or trimmer potentiometer from that Pin to GND. The EFC resistance adjustment range is 0Ω or GND to 20kΩ max with nominal frequency typically occurring in the 3kΩ to 13kΩ range. Customers will be furnished with the applicable EFC resistor value that can be used to set each individual device within ±0.2 ppm of nominal frequency at time of shipment.

4.3.5 Frequency Aging. Aging limits, when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1 ppm for the first year and ±5 ppm for 15 years.

4.3.5.1 Frequency Aging Duration Option. By customer request, the Aging test may be terminated after 15 days if the aging projection is less than the specified aging limit. This is a common method of expediting 30-day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. Vectron's automated aging systems acquire data every four hours, compared to the minimum MIL-PRF-55310 requirement of once every 72 hours. This makes an extensive amount of data available to perform very accurate aging projections. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit then they would continue to the full 30-day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.6 Operating Characteristics. See Tables 2 and 3. Waveform measurement points and logic limits are in accordance with Table 2 and Figure 1 herein. Start-up time to reach 80% output amplitude is 10 msec typical and 30 msec maximum.

4.3.7 Output Load. See Figure 2 herein.

4.3.8 Phase Noise. See Table 2B for typical phase noise.

5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 16th character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that

include MIL-PRF-55310 Group A Testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

(K) Modified MIL-PRF-38534 Class K Screening, Group A QCI and 30-day aging
(F) MIL-PRF-55310, Rev F, Class S Screening, Groups A & B QCI
(S) MIL-PRF-55310, Rev E, Class S Screening, Groups A & B QCI
(C) Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
(B) MIL-PRF-55310, Class B Screening, Groups A & B QCI
(X) Engineering Model (EM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection and test options that can be added by explicit purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):
(E) Enhanced Element Evaluation (MIL-PRF-38534 Rev L for Class K components as specified in DOC208191), 100krad die, Premium Q Swept Quartz
(R) MIL-PRF-38534 Rev K element evaluation for Class K components, 100krad die, Swept Quartz
(B) Class B components, Swept Quartz
(C) Class B components, Non-Swept Quartz
(D) COTS components, Non-Swept Quartz

b. Input Voltage as the 15th character
c. Not Used
d. Radiographic Inspection
e. Group C Inspection: MIL-PRF-55310 Rev E (requires 8 destruct specimens)
f. Group C Inspection: MIL-PRF-55310, Rev F (requires 8 destruct specimens, includes Random Vibration, MIL-STD-883, Method 1014 Leak Test and Life Test)
g. Group C Inspection: In accordance with MIL-PRF-38534, Table C-Xc, Condition PI (requires 8 destruct specimens – 5 pc. Life, 3 pc. RGA). Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Condition C.
h. Internal Water-Vapor Content (RGA) samples and test performance
i. MTBF Reliability Calculations
j. Worst Case Circuit Analysis (unless otherwise specified, MIL-HDBK-1547)
k. Derating and Thermal Analysis (unless otherwise specified, MIL-HDBK-1547 with Tj Max = +105°C; Case Temperature = +85°C)
l. Process Identification Documentation (PID)
m. Customer Source Inspection (pre-cap / final)
n. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Vectron DOC203982.
o. Qualification: In accordance with MIL-PRF-55310, Rev F, Table IV (requires 16 destruct specimens).
p. Qualification: In accordance with EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)
q. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum)
r. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping.

s. As Designed Parts, Materials and Processes List

5.2.1 NASA EEE-INST-002. A combination of Design Pedigree R, Option F Screening, and Qualification per EEE-INST-002, Section C4, Table 3 meet the requirements of Level 1 and Level 2 device reliability.

5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.4 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices (except devices with Screening Option X):

a. Completed assembly and Screening lot travelers & Screening data, including radiographic images, rework history and Certificate of Conformance.
b. Electrical test variables data, identified by unique serial number.
c. Special items when required by purchase order such as Frequency-Temperature Slew plots, Group C data, RGA data.
d. Traceability, component LAT & enclosure LAT and RLAT (if specifically requested on the purchase order).

5.5 Discrepant Material. All MRB authority resides with the procuring activity.

5.6 Failure Analysis. Any failure during Qualification or Group C Inspection will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

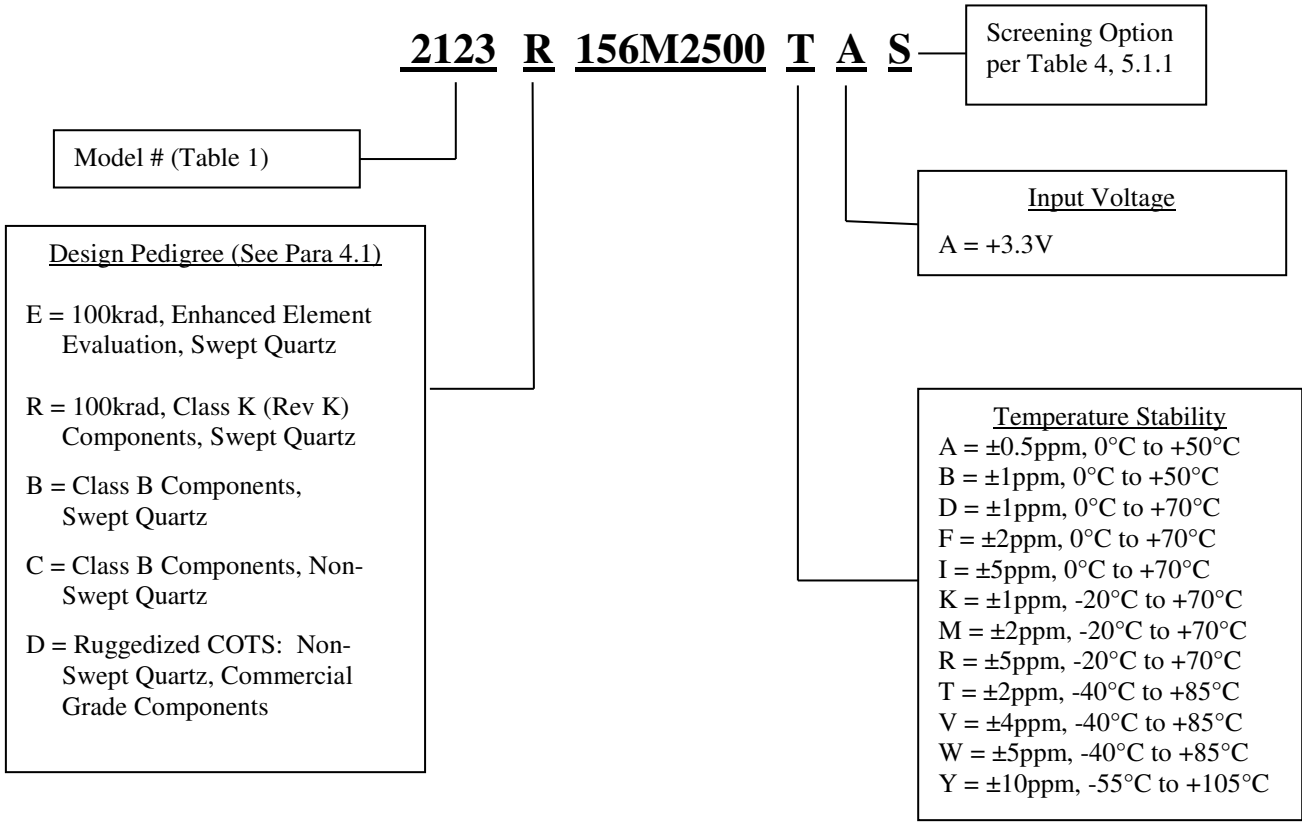
6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling, ESD and transit damage during shipping.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 16 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (¶ 5.2a and b), are included within the device part number.

The Part Number breakdown is described as:



7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.

7.1.2 Design Pedigree. Class S designs correspond to letters "E" and "R" and are described in paragraph 5.2a. Class B variants correspond to either letter "B" or "C" and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, correspond to letter "D".

7.1.2.1 Input Voltage. Voltage is the 15th character. Voltage availability is dependent on platform.

7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

7.1.4 Screening Options. The 16th character is the Screening Option selected from Table 4.

7.2 Optional Design, Test and Data Parameters. Test and documentation requirements above that of the standard high reliability model shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru-s).

MODEL #	PACKAGE	OUTPUT (LVDS)	MECHANICAL OUTLINE AND I/O CONNECTIONS
2123	24 Lead Flatpack	Single Pair	Figure 3
2223 1/	24 Lead Flatpack	Single Pair	Figure 4
2133	24 Lead Flatpack	Dual Pair	Figure 5
2233 1/	24 Lead Flatpack	Dual Pair	Figure 6

1/. Model 2223 and 2233 represent lead formed versions.

TABLE 1 - Item Identification and Package Outline

Models 2123, 2223, 2133, 2233				
Supply Voltage: +3.3V ±5%				
Single-Ended Output Voltage ($+V_{OD}$ or $-V_{OD}$): 250mV to 450mV				
Differential Output Voltage (V_{Diff}): 500mV to 900mV				
Offset Voltage (V_{OS}): 1.125V to 1.450V				
Frequency Range (MHz)	Max Current (Vcc Osc Input) (mA) 1/	Max Current (Vcc LVDS Chip) (mA) 1/	Max t_r/t_f (ps) 2/	Duty Cycle (%) 2/
10 - 200	25	20	600	40 to 60

1/. Current measurements are taken at maximum supply voltage.
2/. Waveform measurement points and logic limits are in accordance with Figure 1.

TABLE 2 - Electrical Performance Characteristics

Frequency (MHz)	Typical Period Jitter 1 sigma (ps)	Typical Period Jitter peak-to-peak (ps)	Typical Phase Jitter 12kHz to 20MHz (ps)
136	3.5	24	0.15

TABLE 2A – Typical Jitter Performance

TABLE 2B – Typical Phase Noise at 136 MHz

OPERATION LISTING	REQUIREMENTS AND CONDITIONS
Input Current	MIL-PRF-55310, Para 4.8.5.1
Initial Accuracy @ Ref. Temp.	MIL-PRF-55310, Para 4.8.6
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22
Duty Cycle	MIL-PRF-55310, Para 4.8.23
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4 except the max voltage shall be +3.60 VDC.
Initial Freq. – Temp. Accuracy	MIL-PRF-55310, Para 4.8.10.1
Freq. – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14
Start-up Time (fast/slow start)	MIL-PRF-55310, Para 4.8.29

TABLE 3 - Electrical Test Parameters

OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option K	Option F	Option S	Option C	Option B	Option X
	SCREENING	MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)	M38534K K	M55310F S	M55310E S	M55310F B+	M55310F B	EM
1	Non-Destruct Bond Pull	MIL-STD-883, Meth 2023	X	X	X	NR	NR	NR
2	Internal Visual	MIL-STD-883, Meth 2017 Class K or H, Meth 2032 Class K or H	X K	X K	X K	X H	X H	X H
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.
4	Random Vibration	MIL-STD-883, Meth 2026, Cond I-B, 15 mins in each axis	NR	X	NR	NR	NR	NR
5	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	X	X	X	NR	NR	NR
6	Temperature Cycle	MIL-STD-883, Meth 1010, Cond. B, 10 cycles min.	X	NR	X	X	X	NR
		MIL-STD-883, Meth 1010, Cond. C, 10 cycles min.	NR	X	NR	NR	NR	NR
7	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	X	X	X	X	NR
8	Particle Impact Noise Detection	MIL-STD-883, Meth 2020, Cond B	X	NR	X	X	NR	NR
		MIL-STD-883, Meth 2020, Cond A	NR	X	NR	NR	NR	NR
9	Electrical Testing, Pre Burn-In	Nominal Vcc, +25°C	X	X	X	X	X	X
10	1st Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	X 240 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	NR
11	Electrical Testing, Intermediate	Nominal Vcc, +25°C & Op Temp Extremes	X	NR	NR	NR	NR	NR
12	2nd Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	NR	NR	NR	NR	NR
13	Electrical Testing, Post Burn-In	Nominal Vcc & extremes, nominal temperature & extremes	X	X	X	X	X	NR
14	Seal: Fine Leak	MIL-STD-202, Meth 112, Cond C, 5 x 10^{-8} atm cc/sec max	X	NR	X	X	X	X
		MIl-STD-883, Meth. 1014, TC A2 or B1	NR	X	NR	NR	NR	NR
15	Seal: Gross Leak	MIL-STD-202, Meth 112, Cond D	X	NR	X	X	X	X
		MIL-STD-883, Meth. 1014, TC B2 or B3	NR	X	NR	NR	NR	NR
16	Radiographic Inspection	MIL-STD-883, Meth 2012	X	X	X	X	NR	NR
17	Solderability	MIL-STD-883, Meth 2003	1/	1/	1/	1/	1/	1/
18	External Visual Inspection	MIL-STD-883, Method 2009	X	X	X	X	X	NR
19	Group A Electrical Test	MIL-PRF-55310	X	X	X	Sample	Sample	NR
20	Aging, 30 Day 2/ (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	X	X	X	Sample	Sample	NR
21	Group C Inspection (optional)	See Para 5.2 herein for details of supplier recommended Group C Inspection options	Para 5.2(g)	Para 5.2(f)	Para 5.2(e)	Para 5.2(e)	Para 5.2(e)	NR

LEGEND: X = Required, NR = Not Required, AR = As Required

TABLE 4 - Screening & Test Matrix

1/ Performed at package LAT. Include LAT data sheet.

2/ By customer request, the Aging test may be terminated after 15 days if the projected aging rate is meeting the specification requirements as described in paragraph 4.3.5.1 herein. Must be explicitly stated on the customer PO.

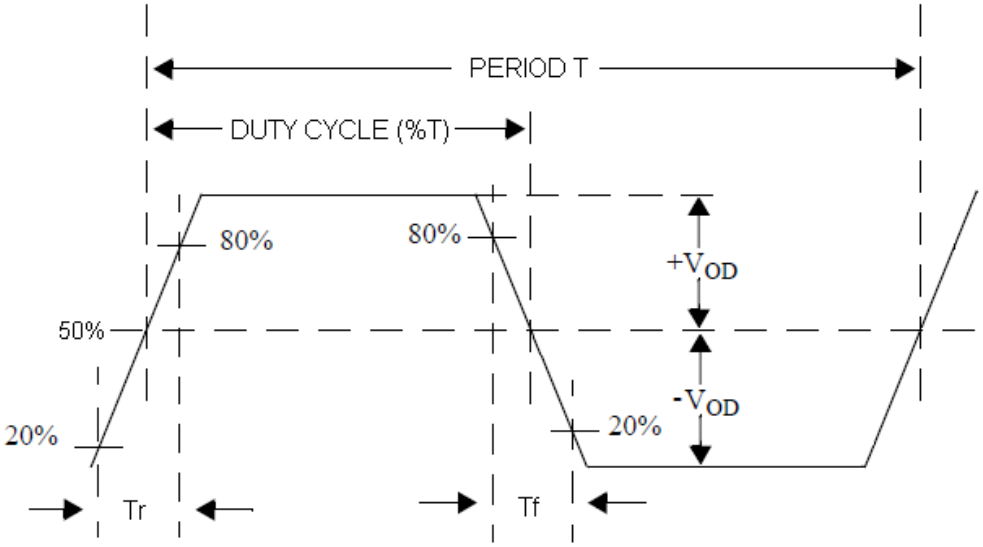


Figure 1
Differential Output Waveform

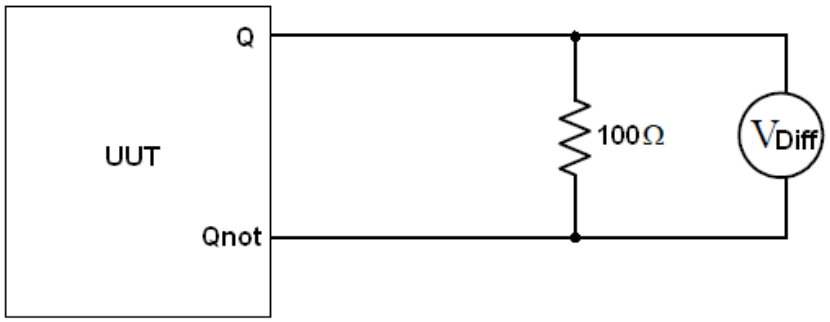


Figure 2
Output Load

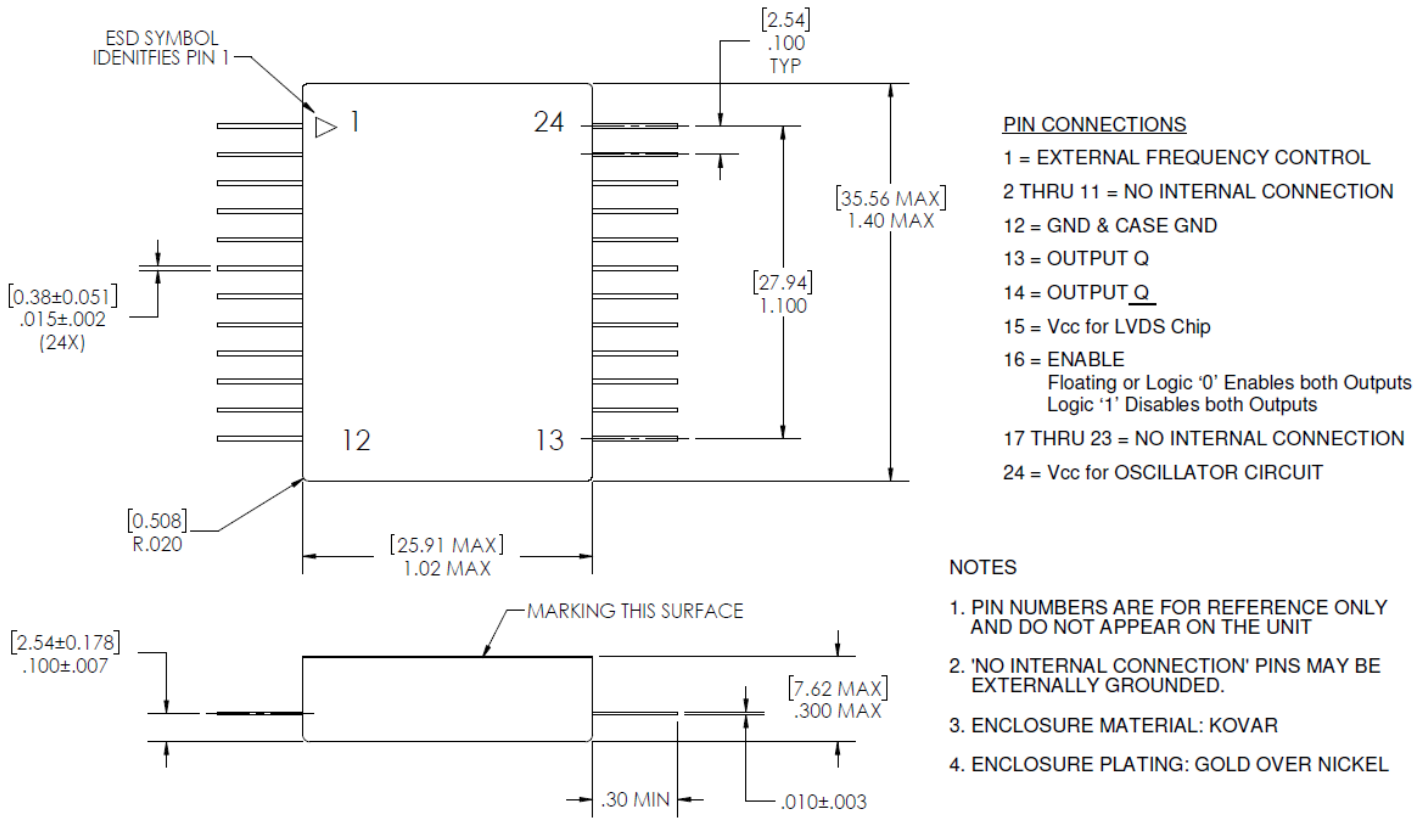
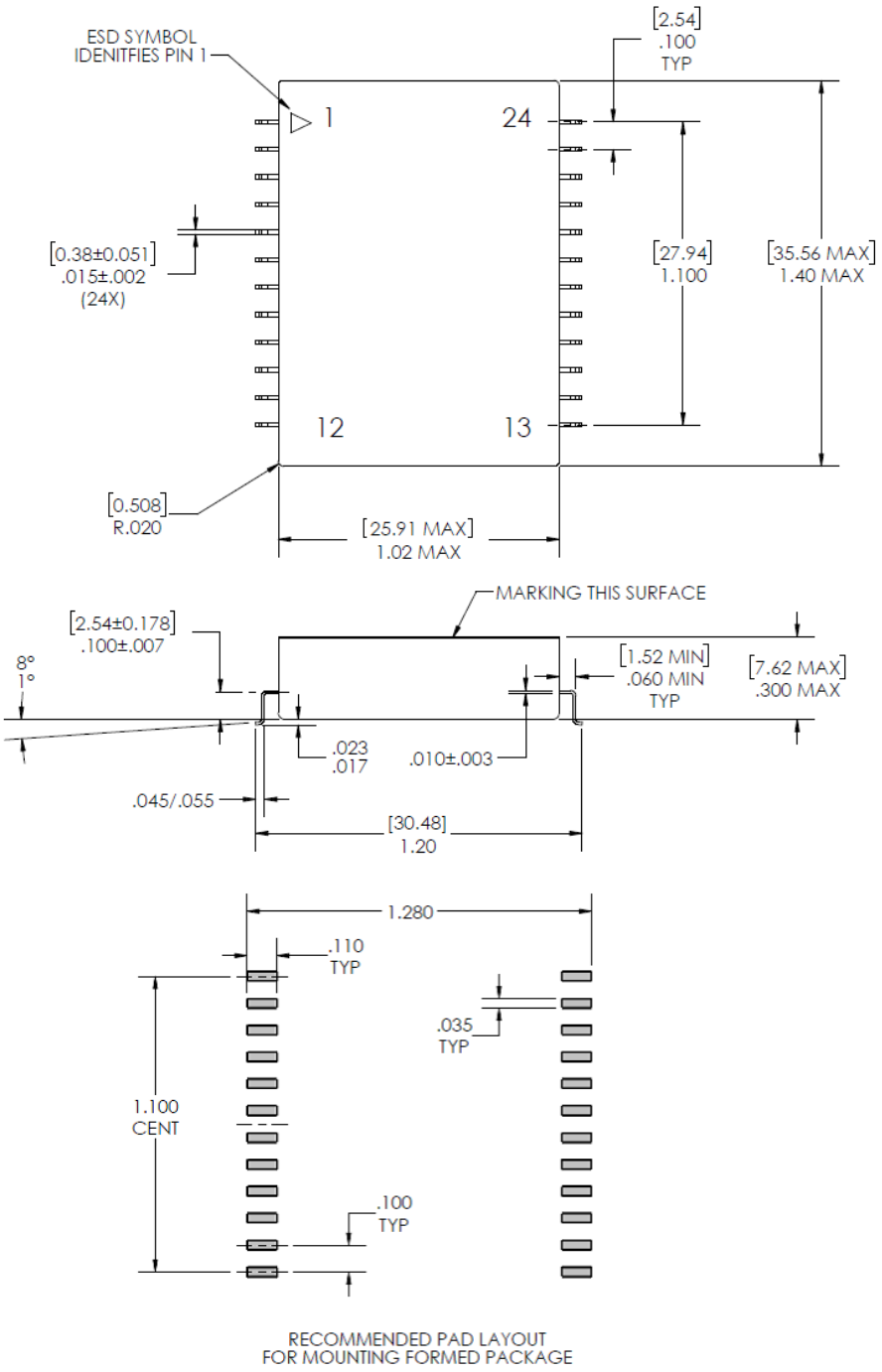


FIGURE 3 Single LVDS pair
Models 2123 Package Outline



PIN CONNECTIONS

1 = EXTERNAL FREQUENCY CONTROL

2 THRU 11 = NO INTERNAL CONNECTION

12 = GND & CASE GND

13 = OUTPUT Q

14 = OUTPUT $\overline{Q}$

15 = Vcc for LVDS Chip

16 = ENABLE
Floating or Logic '0' Enables both Outputs
Logic '1' Disables both Outputs

17 THRU 23 = NO INTERNAL CONNECTION

24 = Vcc for OSCILLATOR CIRCUIT

NOTES

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE UNIT
2. 'NO INTERNAL CONNECTION' PINS MAY BE EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL

FIGURE 4 Single pair LVDS
Models 2223 Package Outline

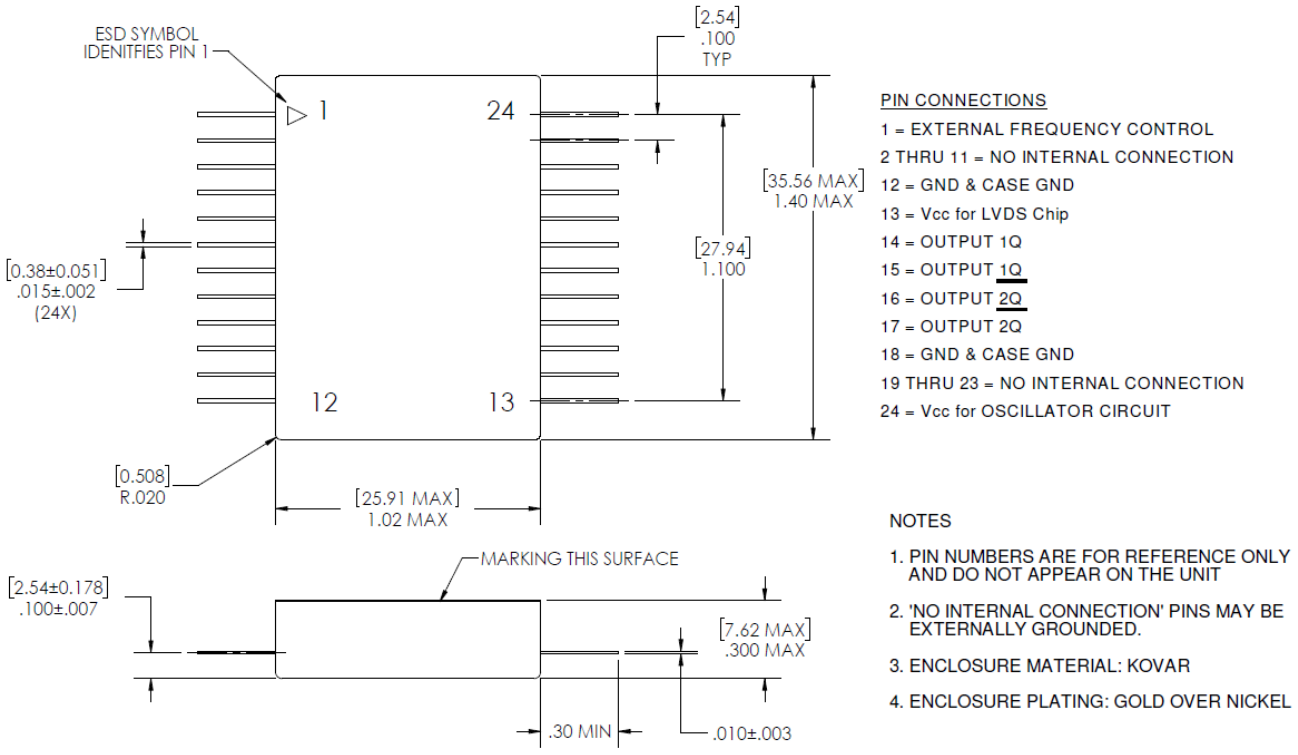


FIGURE 5 Dual pair LVDS
Models 2133 Package Outline

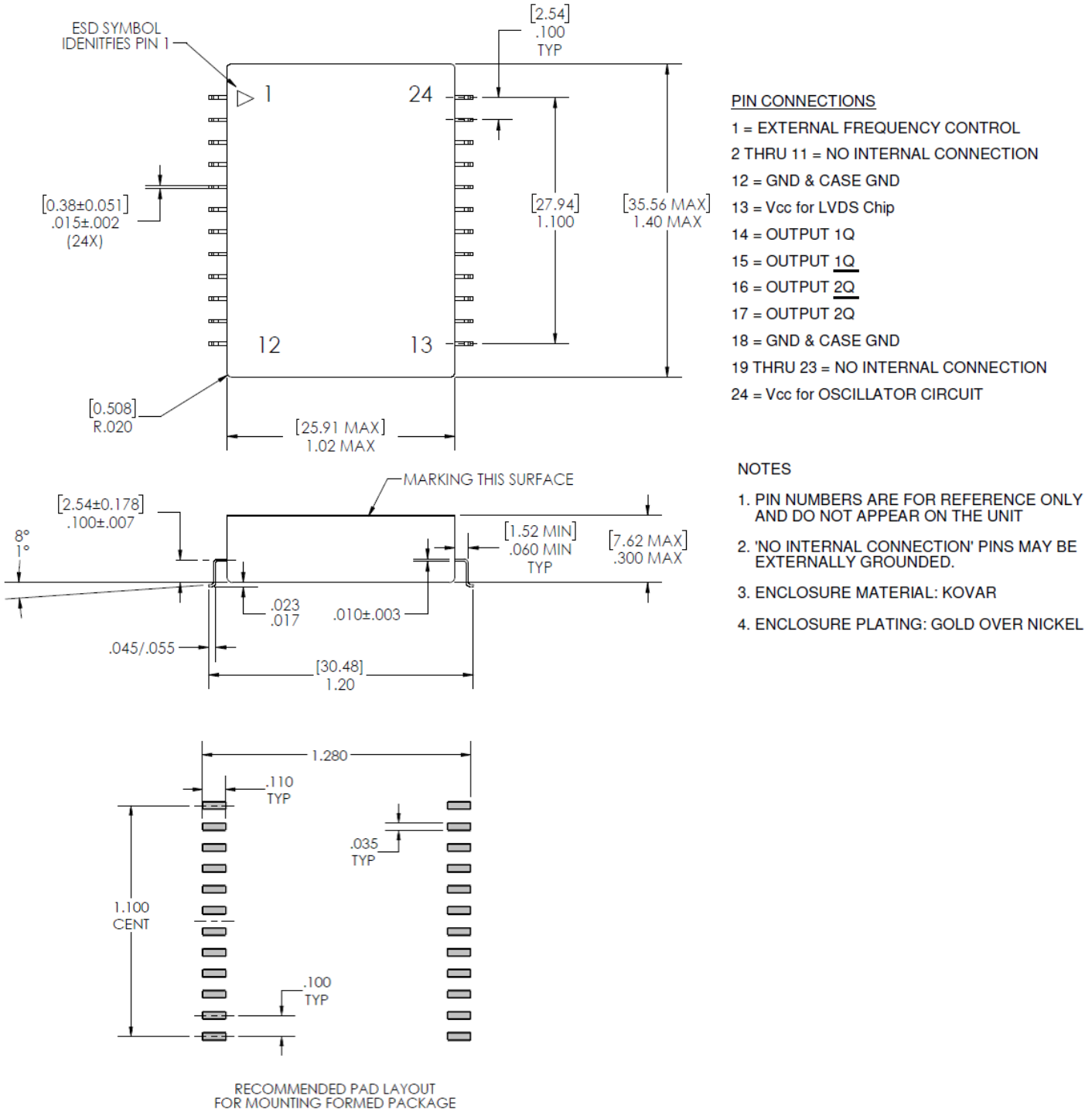


FIGURE 6 Dual pair LVDS
Models 2233 Package Outline

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**DOC207139**	C	**17**