Description

The VS-720 is a Voltage Controlled SAW Oscillator that achieves low phase noise and very low jitter performance. The VS-720 is housed in an industry standard 6-Pad leadless ceramic package that is hermetically sealed. Packaging options include bulk or tape and reel.

Features

- Industry Standard Package, 5.0 x 7.5 x 2.0 mm
- ASIC Technology For Ultra Low Jitter
  - 0.100 ps-rms typical across 12 kHz to 20 MHz BW
  - 0.120 ps-rms typical across 50 kHz to 80 MHz BW
- Output Frequencies from 150 MHz to 1 GHz
- 3.3 V Operation
- LV-PECL or LVDS Configuration with Fast Transition Times
- Up to ± 100 ppm APR
- Complementary Outputs
- Output Disable Feature
- Improved Temperature Stability over Standard VCSO
- Product is free of lead and compliant to EC RoHS Directive

Applications

PLL circuits for clock smoothing and frequency translation

Description	Standard
1-2-4 Gigabit Fibre Channel	INCITS 352-2002
10 Gigabit Fibre Channel	INCITS 364-2003
10GbE LAN / WAN	IEEE 802.3ae
OC-192	ITU-T G.709
SONET / SDH	GR-253-CORE Issue4

Block Diagram

Need A Block Diagram

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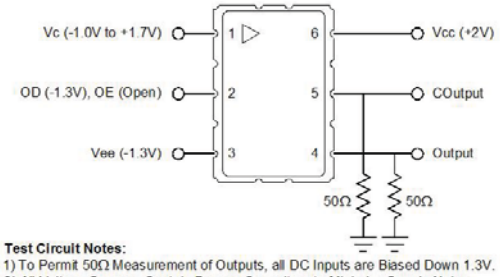
Performance Specifications

Electrical Performance						
Parameter	Symbol	Min	Typical	Maximum	Units	Notes
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}		55	70	mA	3
Frequency						
Nominal Frequency	f_N	150		1000	MHz	1,2,3
Absolute Pull Range (Ordering Option)	APR		±100		ppm	1,2,8
Linearity	Lin			±10	%	2,8
Gain Transfer (See pg 5)	K_V		+90		ppm/V	2,8
Temperature Stability	f_{STAB}		±20		ppm	1
Outputs						
Mid Level - LVPECL		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V	2,3
Swing - LVPECL		450	600	750	mV-pp	2,3
Mid Level - LVDS		V_{CC}-2.4	V_{CC}-2.3	V_{CC}-2.5	V	2,3
Swing - LVDS		250	350	450	mV-pp	2,3
Current	I_{OUT}			20	mA	6
Rise Time	t_R			500	ps	5,6
Fall Time	t_F			500	ps	5,6
Symmetry	SYM	45	50	55	%	2,3
Jitter (12 kHz - 20 MHz BW) 622.08 MHz	ϕJ		0.100	0.250	ps-rms	6,7
Jitter (50 kHz - 80 MHz BW) 622.08 MHz	ϕJ		0.120	0.300	ps-rms	6,7
Period Jitter, RMS (622.08 MHz)	ϕJ		3.0	4.0	ps-rms	9
Period Jitter, Peak - Peak (622.08 MHz)	ϕJ		20	30	ps pk-pk	9
Spurious Suppression			-55		dBc	2
Control Voltage						
Control Voltage Range for APR	V_C	0.3		3.0	V	2,8
Control Voltage Input Impedance	Z_{IN}	75			KΩ	6
Control Voltage Modulation BW	BW	50			kHz	6
Operating Temperature	T_{OP}	0/70, -20/70 or -40/85			°C	1,3
Package Size		5.0 x 7.5 x 2.0			mm	

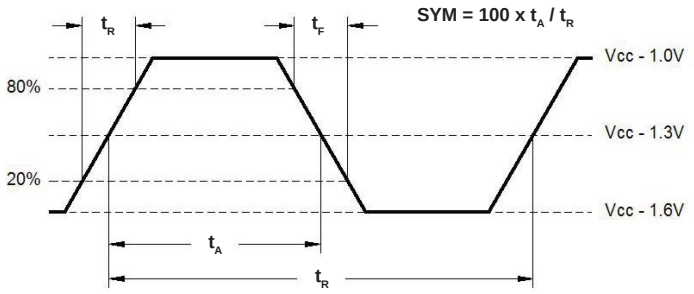
1] See Standard Frequencies and Ordering Information tables (Pg 7) for more specific information
2] Parameters are tested with production test circuit below (Fig 1).
3] Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4] Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5] Measured from 20% to 80% of a full output swing (Fig 2).
6] Not tested in production, guaranteed by design, verified at qualification.
7] Integrated across stated bandwidth per GR-253-CORE Issue4.
8] Tested with Vc = 0.3V to 3.0V unless otherwise stated in part description
9] Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 250K samples taken
10] ±100 ppm APR parts will have linearity of >10%

Fig 1: Test Circuit



Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

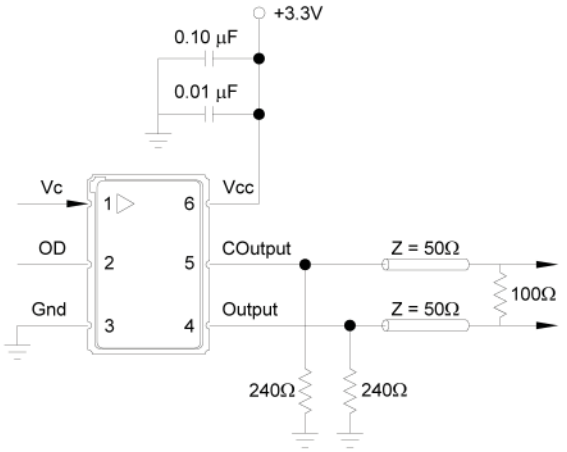
Fig 2: 10K LV-PECL Waveform



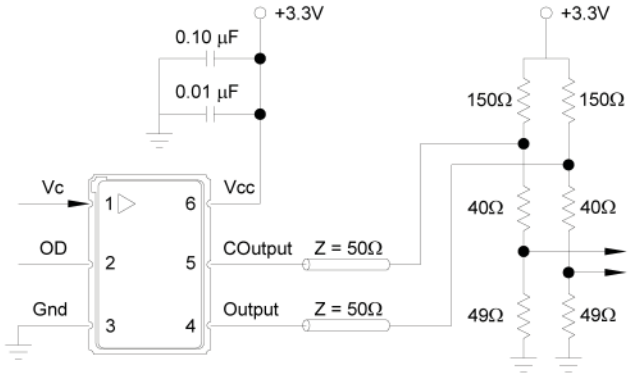
Absolute Maximum Ratings			
Parameter	**Symbol**	**Ratings**	**Unit**
Power Supply	V_{CC}	0 to 4	V
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 40	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

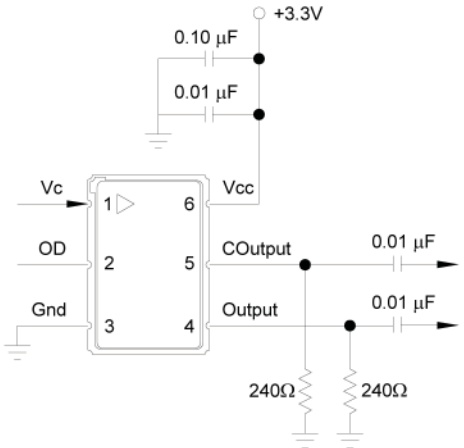
Suggested Output Load Configurations



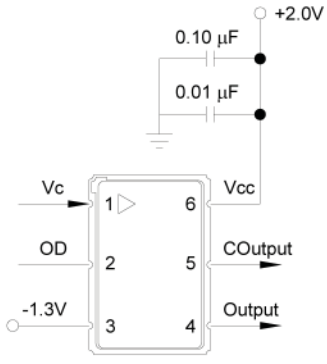
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.

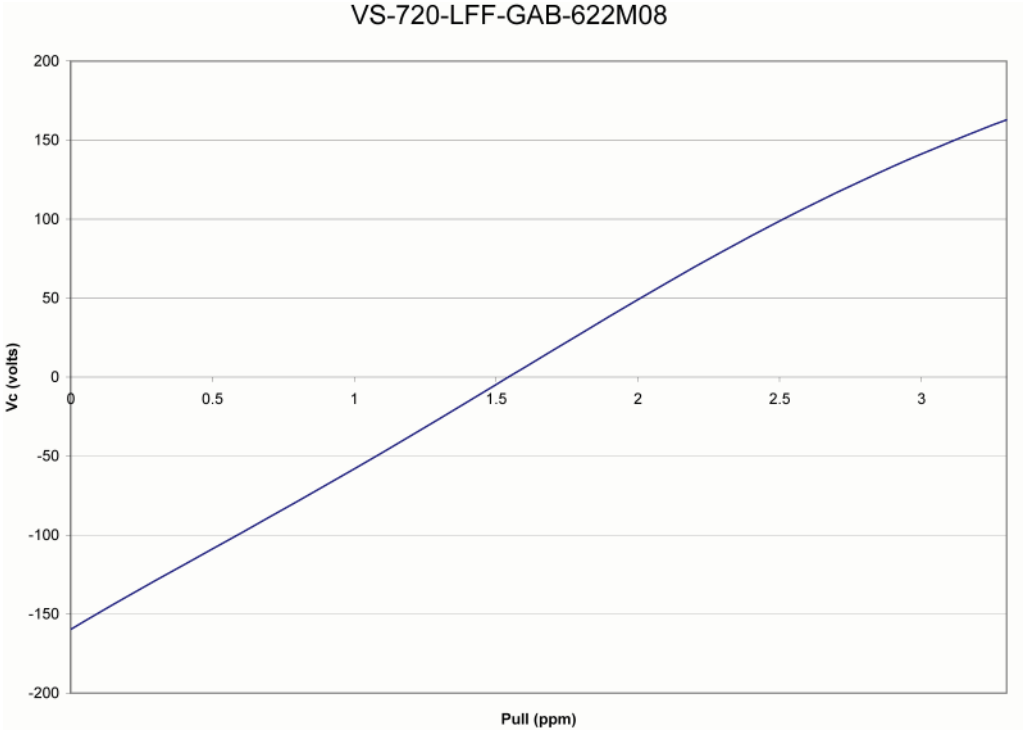


Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.

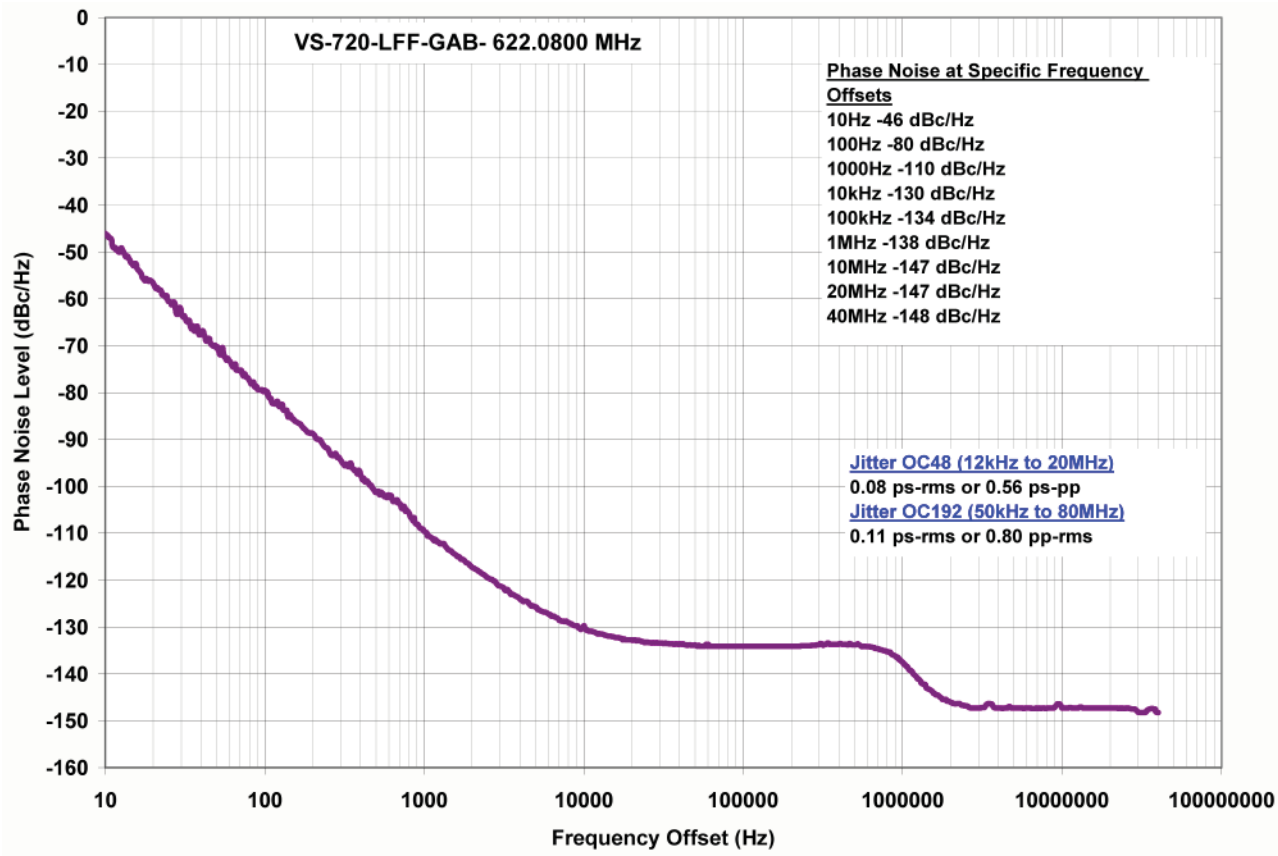


Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplys as shown. Similiar to figure 1.

Typical Characteristics - Gain Transfer



Typical Characteristics - Phase Noise



Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-720 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	**Conditions**
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015

Handling Precautions

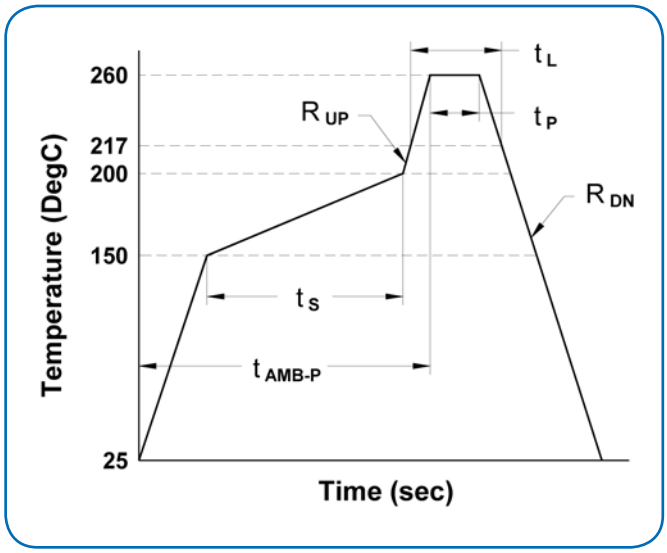
Although ESD protection circuitry has been designed into the VS-720 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	**Minimum**	**Conditions**
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	**Symbol**	**Value**
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

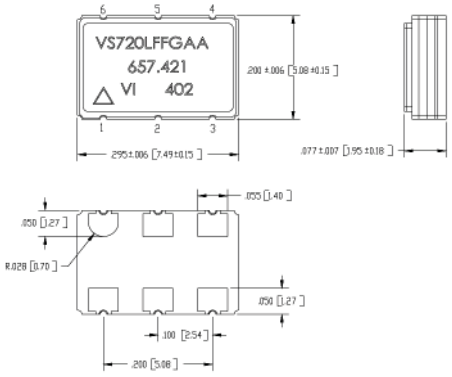
The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VS-720 device is hermetically sealed so an aqueous wash is not an issue.

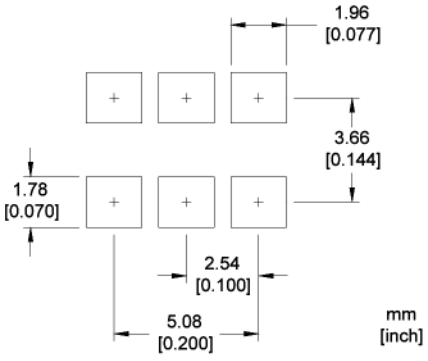
Termination Plating:
Electroless Gold Plate over Nickel Plate



Outline Drawing & Pad Layout

Dimensions in inches (mm)

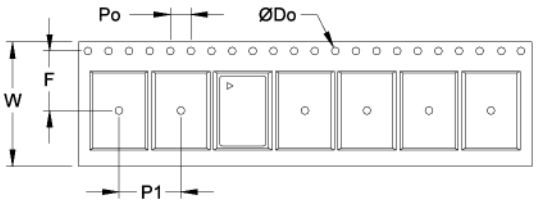


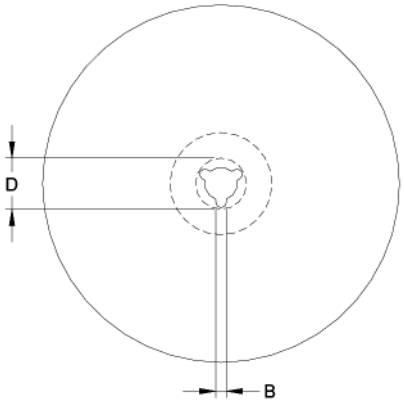


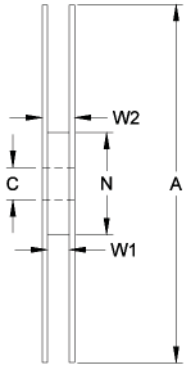
Pin Out		
Pin	**Symbol**	**Function**
1	V_C	VCXO Control Voltage
2	OE[1]	Enable = LV-CMOS logic 0 or Ground Disable = LV-CMOS logic 1 **see Note 1 below**
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{CC}	Power Supply Voltage (3.3V ±10%)

Note 1: For proper operation disable pin can not be left floating.
See page 7 for alternative input logic operation

Tape & Reel (EIA-481-2-A)







Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	
VS-720	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Standard Output Frequencies (MHz)							
*155.5200	*156.2500	*160.0000	*162.0000	*175.0000	*187.5000	*200.0000	212.5000
240.0000	245.7600	250.0000	260.0000	268.8000	300.0000	311.0400	312.5000
320.0000	324.0000	350.0000	375.0000	384.0000	389.6000	400.0000	480.0000
491.5200	500.0000	531.2500	532.0000	533.0000	537.6000	622.0800	625.0000
635.0400	637.5000	640.0000	644.5313	657.4219	666.5143	669.3266	672.1627
690.5692	693.4830	704.3806	707.3527	720.0000	742.4347	768.000	796.8750
800.0000	901.1200	1000.000					

Frequencies not shown are available upon request. *VC-710 is preferred VCXO for frequencies ≤ 200 MHz

Ordering Information

VS - 720 - L F F - G A A - xxx.xxxx

Product Family
VS: VCSO

Package
720: 5 x 7.5 x 2.0 mm
6 Pad Ceramic SMD

Input
L: 3.3 Vdc ±10%

Output
F: LV-PECL (45/55% Symmetry)
P: LVDS (45/55% Symmetry)

Operating Temperature
C: 0°C to 70°C
D: -20°C to 70°C
F: -40 to 85 °C

Absolute Pull Range Options
C: ± 20 ppm minimum
F: ± 32 ppm minimum
G: ± 50 ppm minimum
N: ± 80 ppm minimum
**H: ± 100 ppm minimum

Enable/Disable Input Logic (LV-CMOS)
A: Pin 2 = Enable Low (or Gnd)/Disable High
B: Pin 2 = Enable High (or Vcc)/Disable Low

Performance Options*
A: Default Option
B: Lowest Phase Noise
C: ±5% maximum Linearity
D: ±20ppm maximum Temperative Stability

Frequency (See Above)
150 - 1000 MHz

Example: VS-720-LFF-GBD-622.0800

*Not all combinations are possible

**Linearity >10% for ±100 ppm APR option

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